

FM9B HANKS Intel UMA

VER : 3A

PWA:

PWB:

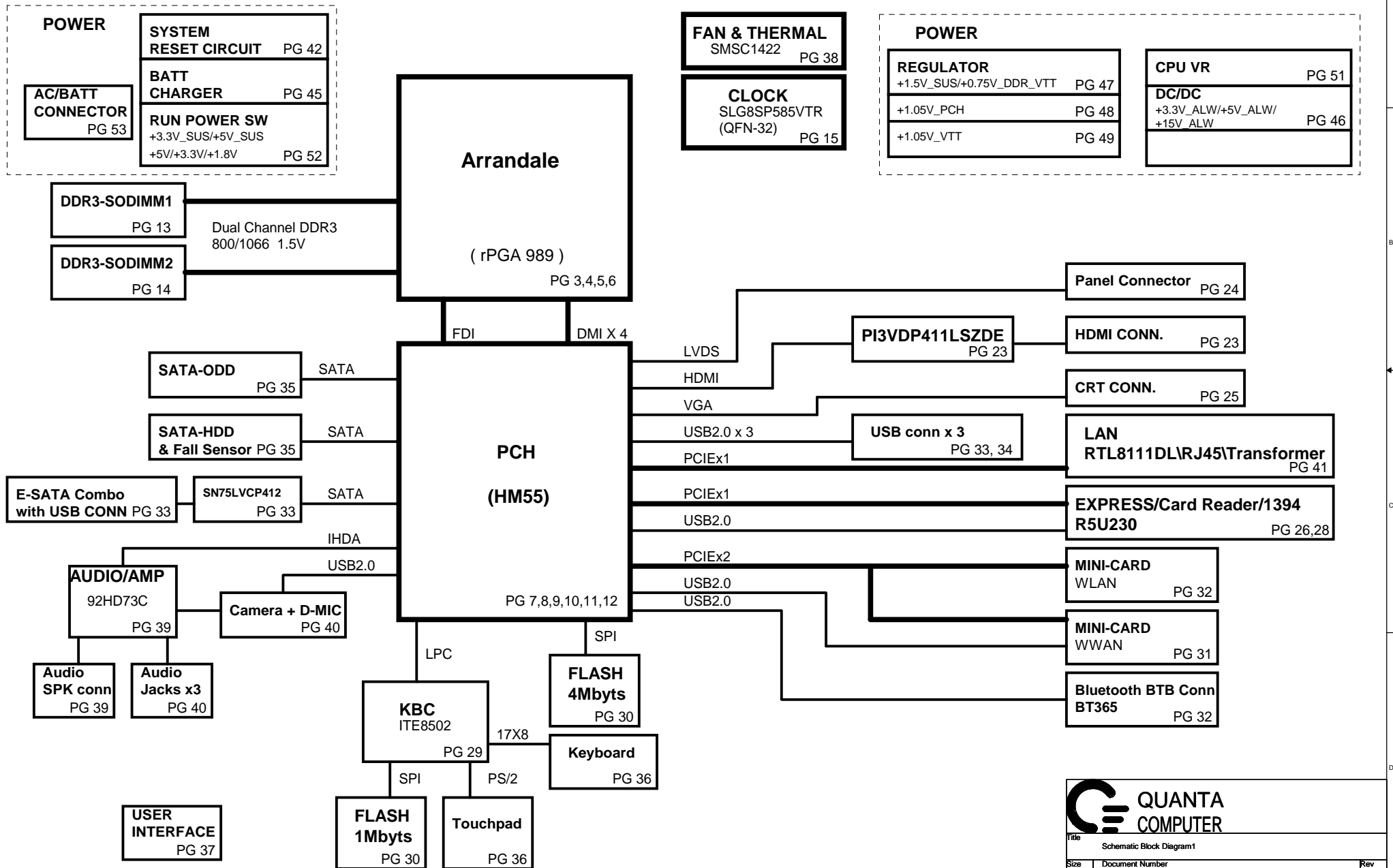



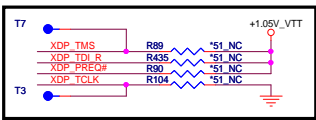
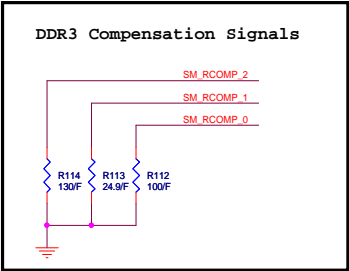
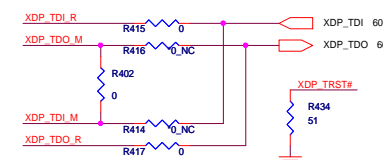
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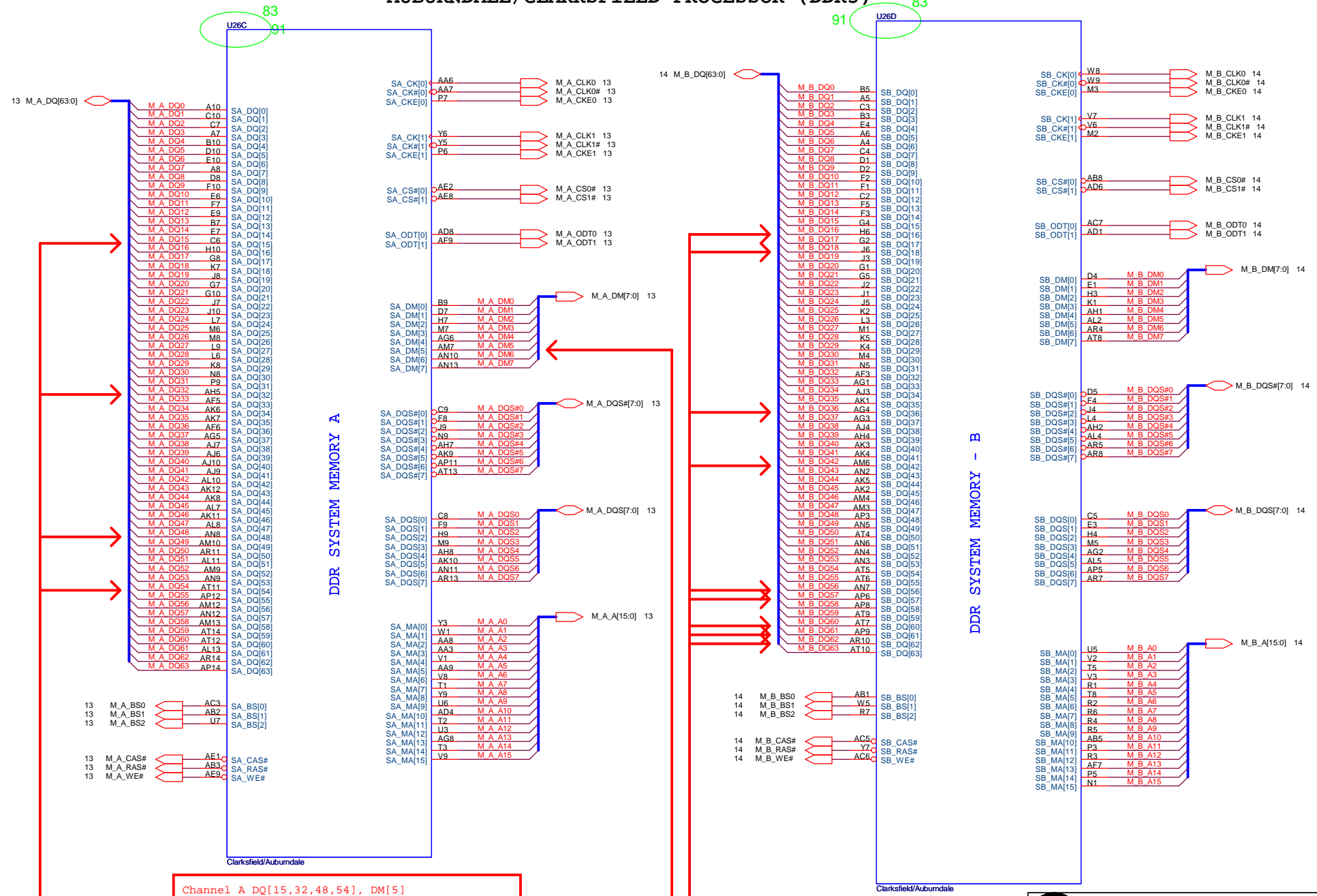
Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,30,45,46,47,48,49,50,51	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	08,11,29,30	RTC		S0~S5
+5V_ALW2	+5V	37,46,52,53	LARGE POWER	MAIN POWER	S0~S5
+5V_ALW	+5V	13,33,44,46,47,48,49,50,51,52	LARGE POWER	ALW_ON	S0~S5
+3.3V_ALW	+3.3V	29,30,35,36,37,42,44,45,46,47,51,52,53	8051 POWER	3.3V_ALW_ON	S0~S5
+5V_SUS	+5V	11,33,34,37,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	07,08,09,10,11,13,14,19,24,28,29,37,41,42,44,48,49,50,52	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.5V	03,05,13,14,47,50,52	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	13,14,47,52	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	11,18,24,25,35,36,38,39,40,51,52	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,7,8,9,10,11,13,14,15,17,24,25,26,28,29,30,31,32,33,35,37,38,39,40,41,42,46,51,52,60	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	05,11,44,52	SDVO POWER	RUN_ON	
+1.05V_VTT	+1.1V	03,05,10,11,49,60	CPU POWER	RUN_ON	
+1.5V_RUN	+1.5V	11,28,31,32,52	Express Card/Min Card	RUN_ON	
+5V_HDD	+5V	35	HDD Power	HDDC_EN	
+1.05V_PCH	+1.05V	08,09,11,15,48	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.77V	05,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	24	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	35	MOD Power	MODC_EN	

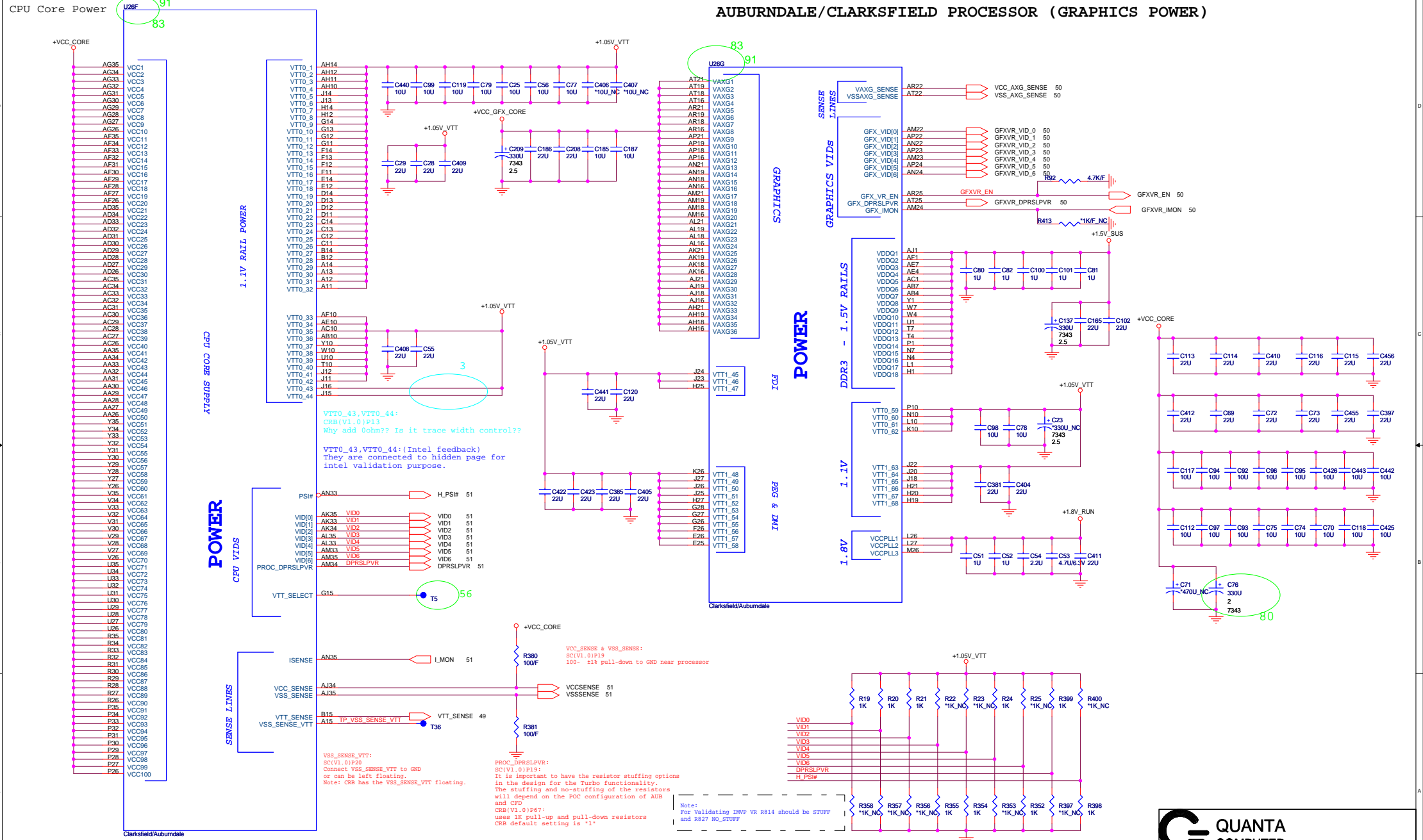
GND PLANE	PAGE	DESCRIPTION
 GND	ALL	



AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



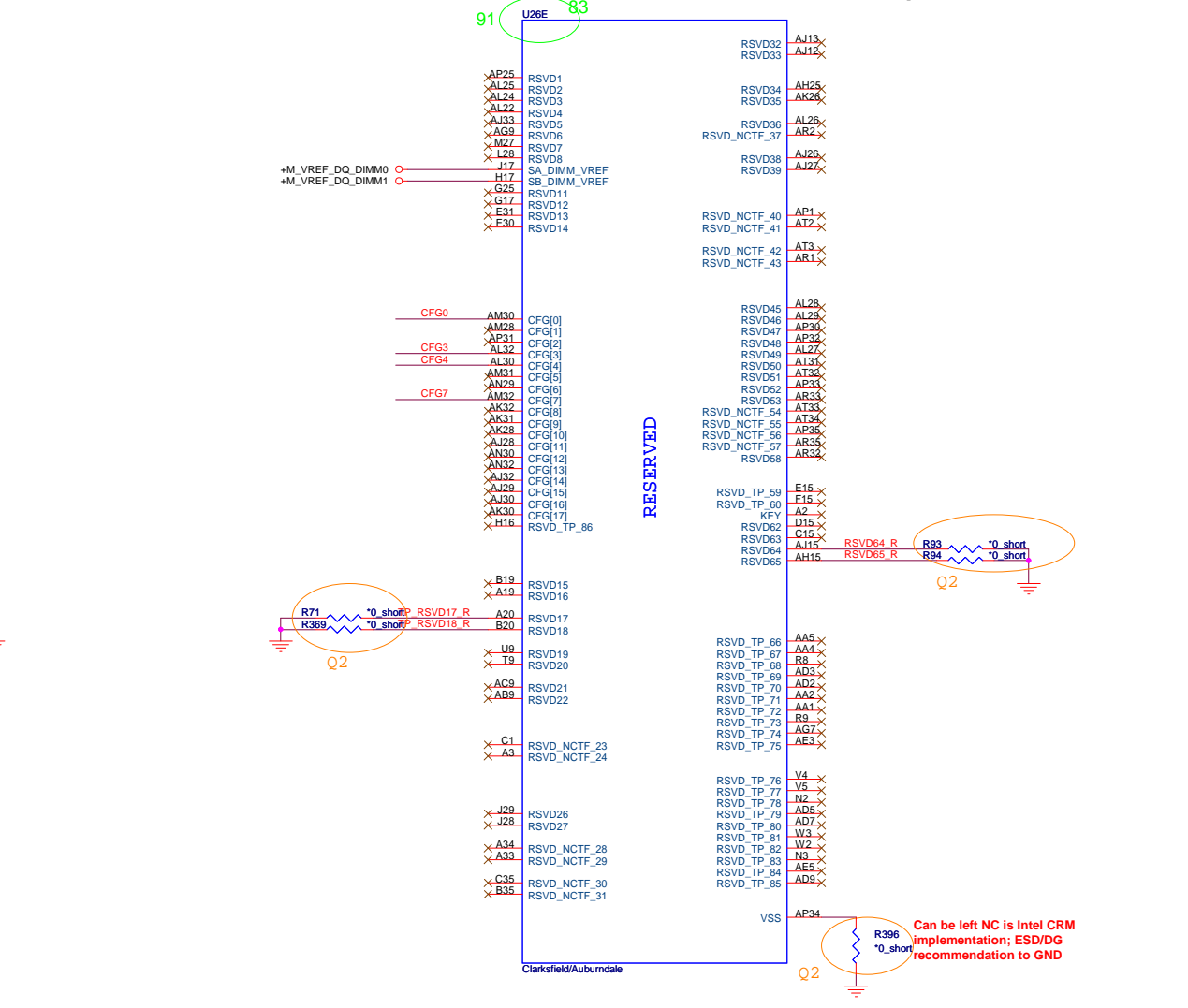
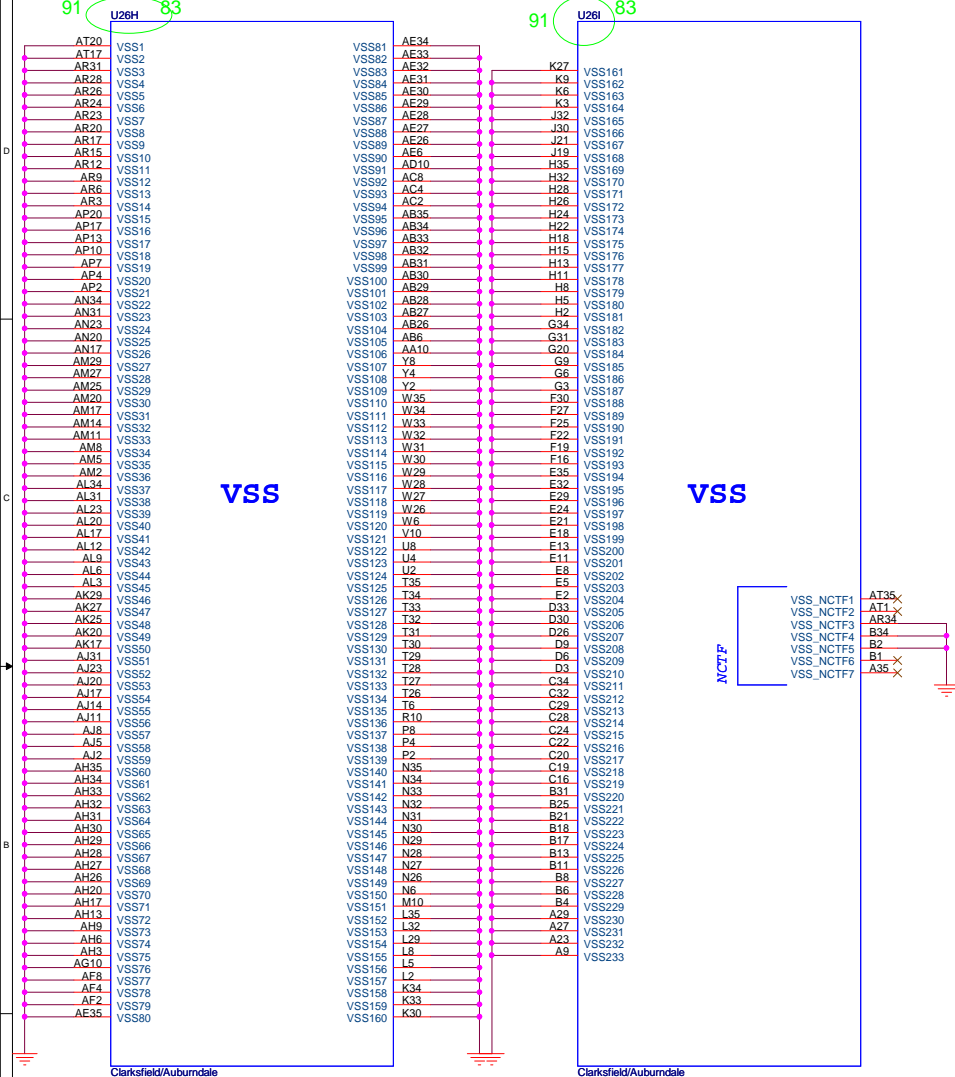
AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)



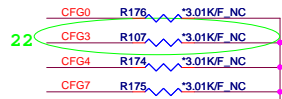
AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



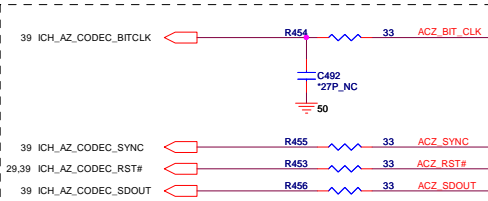
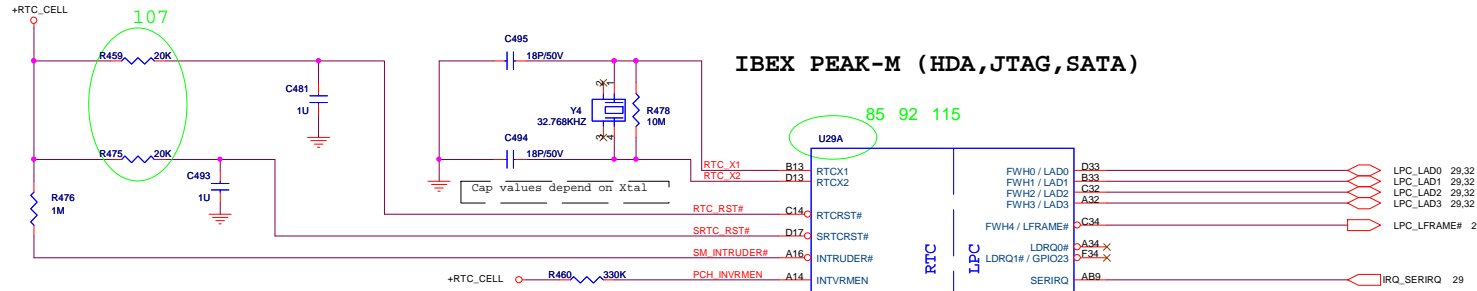
The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

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IBEX PEAK-M (HDA,JTAG,SATA)



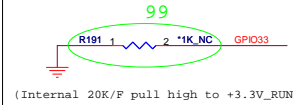
Place all series terms close to PCH except for SDIN input lines, which should be close to source. Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.



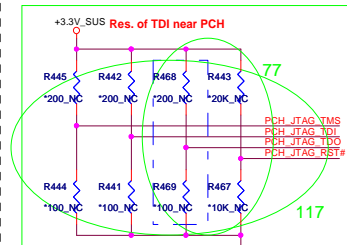
No Reboot strap.	
SPKR	Low = Default. High = No Reboot.

INTVRMEN (Internal Voltage Regulator Enable) : This signal enables the internal 1.05 V regulators. This signal must be always pulled-up to VccRTC.

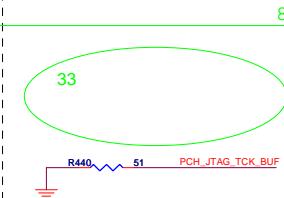
Flash Descriptor Security Override	
GPI033	Low = Enabled High = Disabled



Note : GPI033 is a signal used for Flash Descriptor Security Override/ME Debug Mode. This signal should be only asserted low through an external pull-down in manufacturing or debug environments ONLY.



NC all Res. when PCH is production stage.
Res. of TDO PCH ES1 stage : NC
PCH ES2 stage : pop



Note : Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.



JTAG Test Pads are need to put on the same side of mother board.

SATA port 2/3 are not support in HM55 . They are only in PM 55

SATA HDD

SATA ODD

E-SATA

Distance between the PCH and cap on the "P" signal should be identical distance between the PCH and cap on the "N" signal for the same pair.

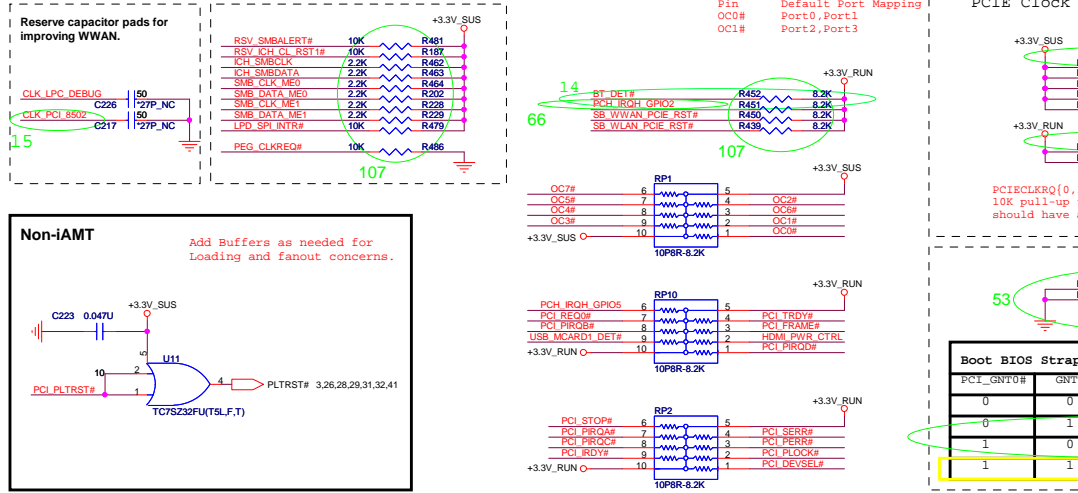
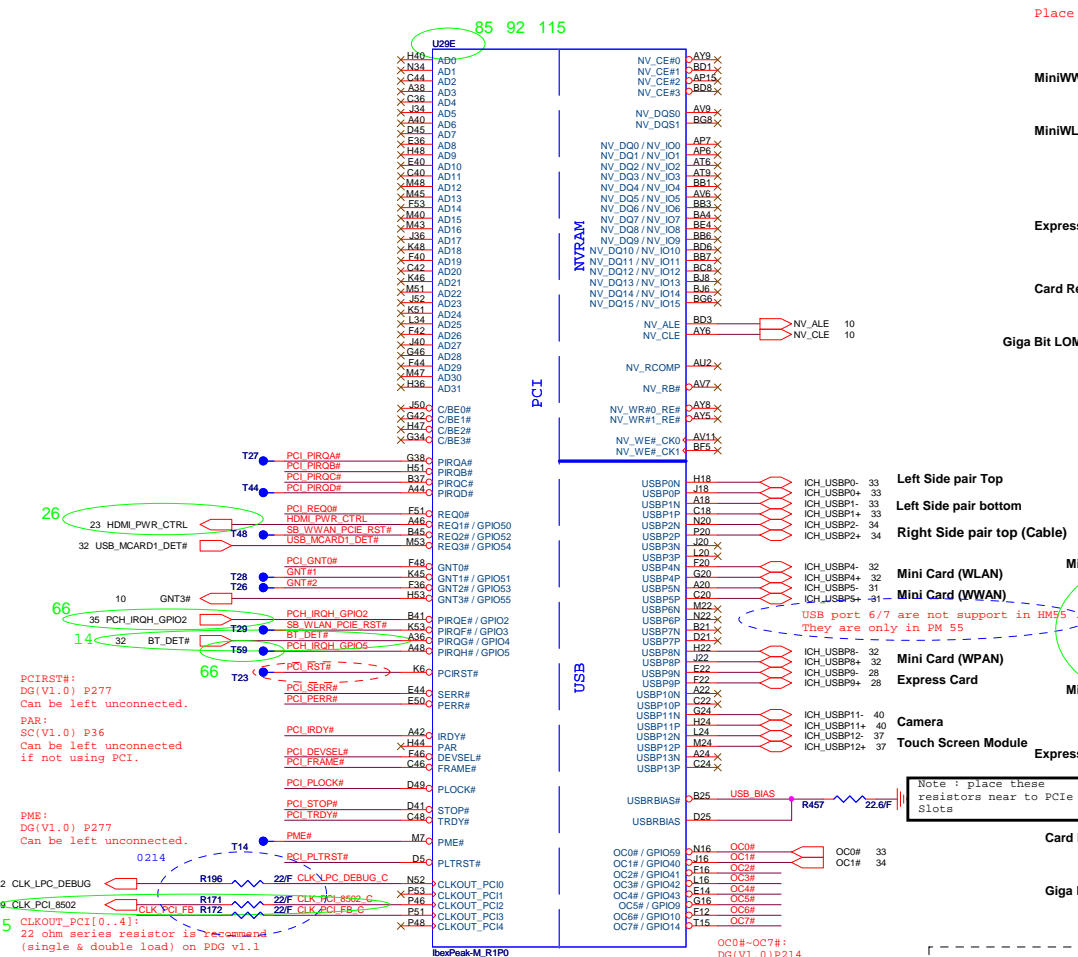


IBEX PEAK-M 1/6

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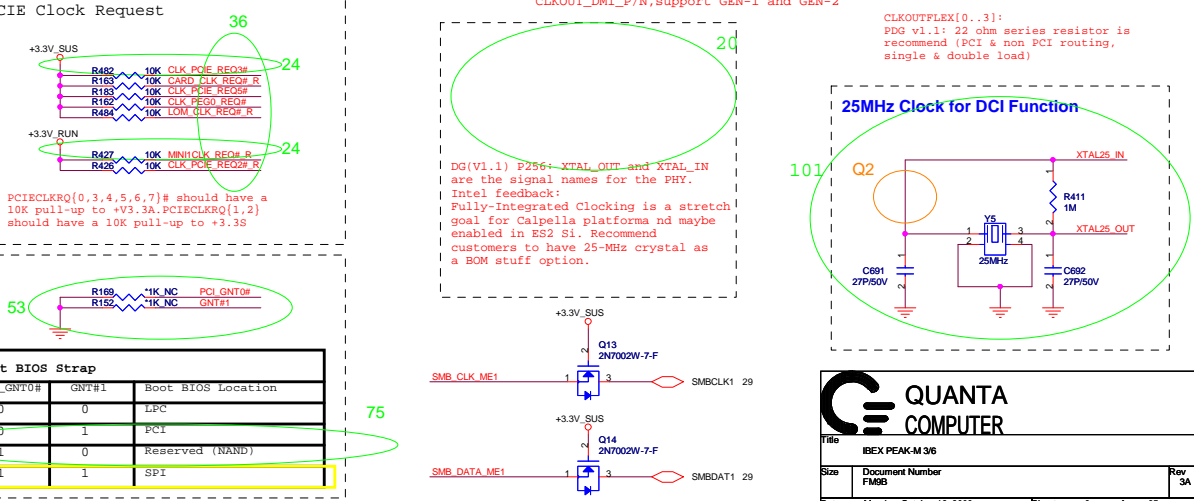
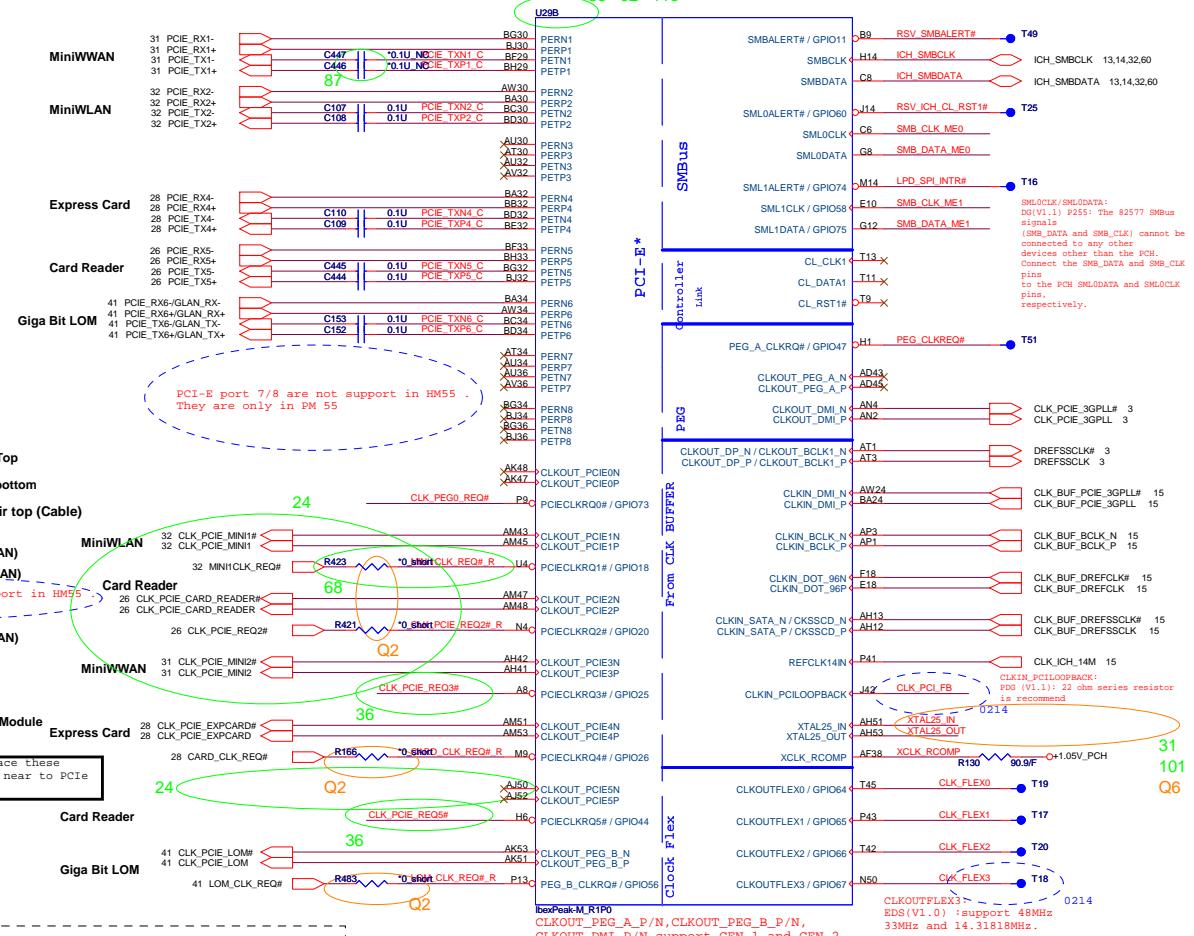
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IBEX PEAK-M (PCI,USB,NVRAM)

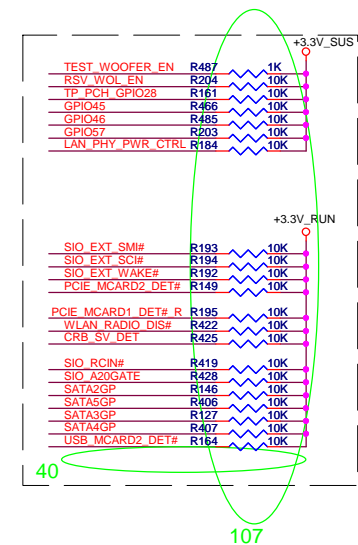


IBEX PEAK-M (PCI-E, SMBUS, CLK)

Place TX DC blocking caps close PCH.



85 92 115



DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

+NVRAM_VCCQ

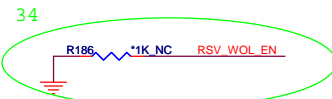
9 NV_ALE 

9 NV_CLE 

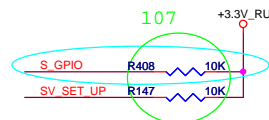
Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable



A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default



Integrated Clock Chip Enable (Reserve to validate for future platforms)	
RSV_WOL_EN	Enable when sampled low Disable when sampled high



SV_SET_UP	1-X High = Strong (Default)
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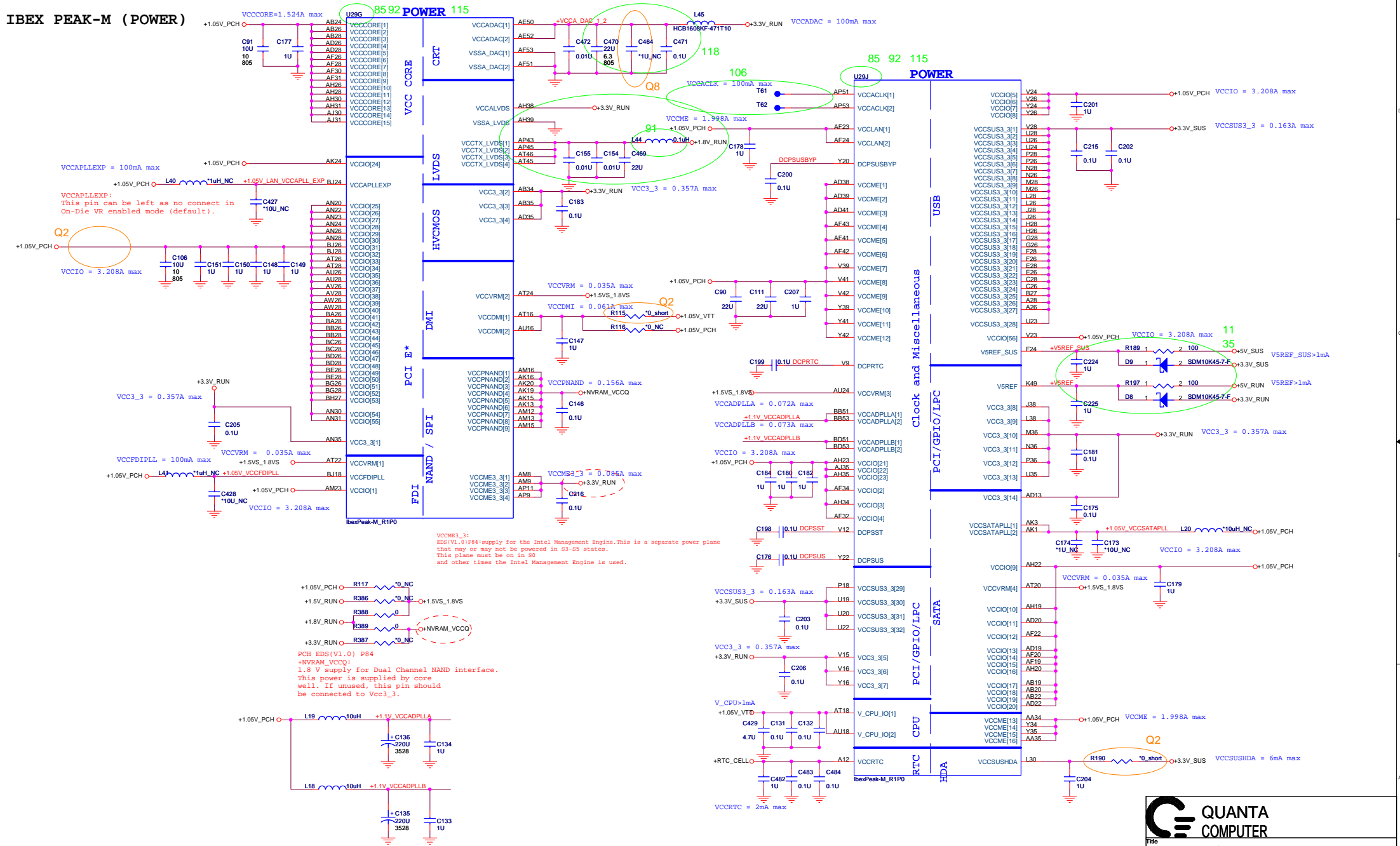
BMBUSY#:
If not used, require a weak pull-up (8.2- K Ω to 10 k Ω) to Vcc3_3.
CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

BMBUSY#:(Intel feedback)
Follow CRB checklist, 1K is
for intel BIOS validation purpose.



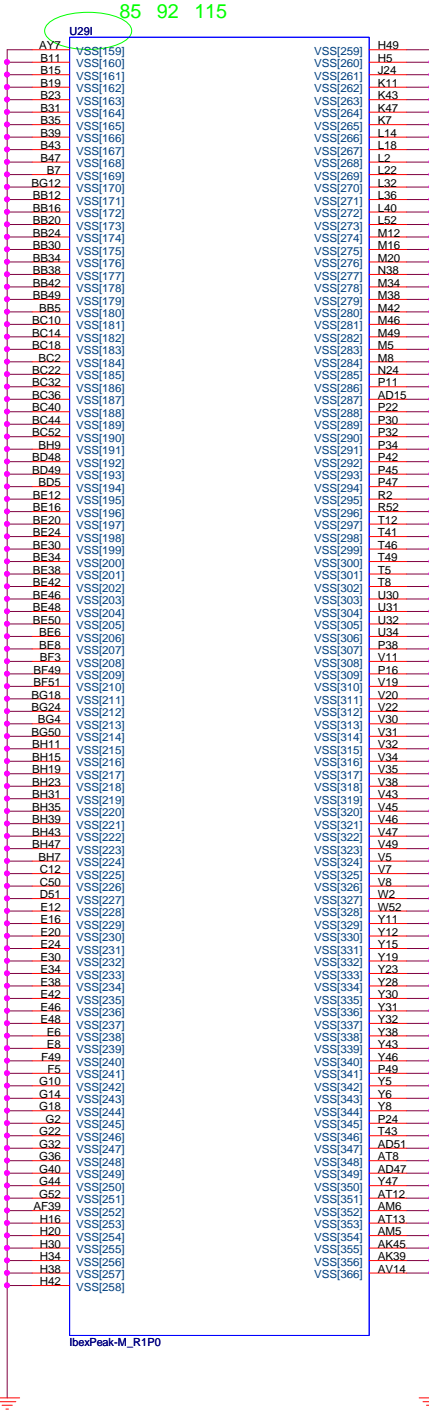
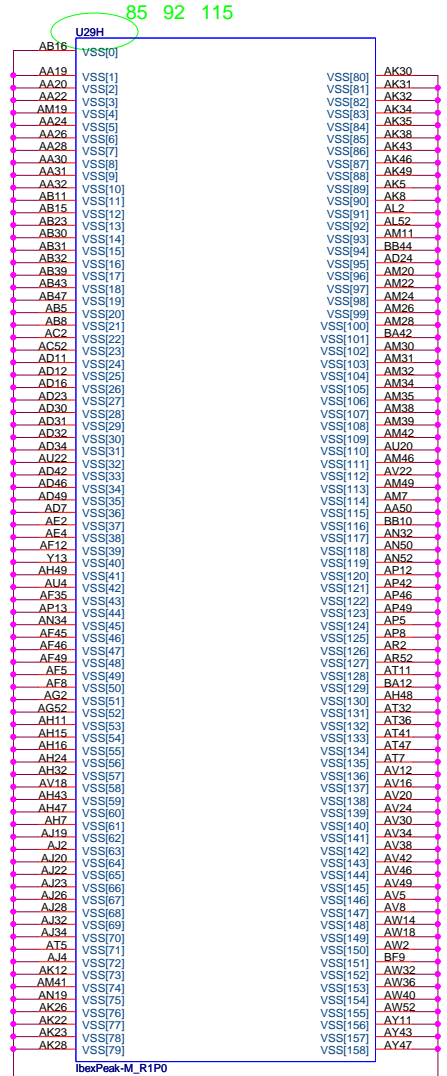
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IBEX PEAK-M (POWER)

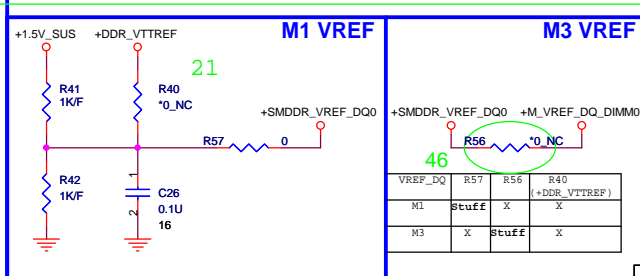


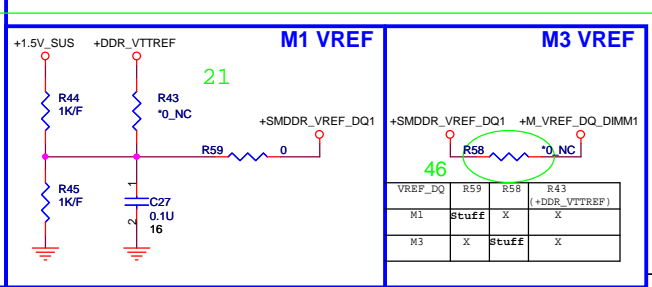
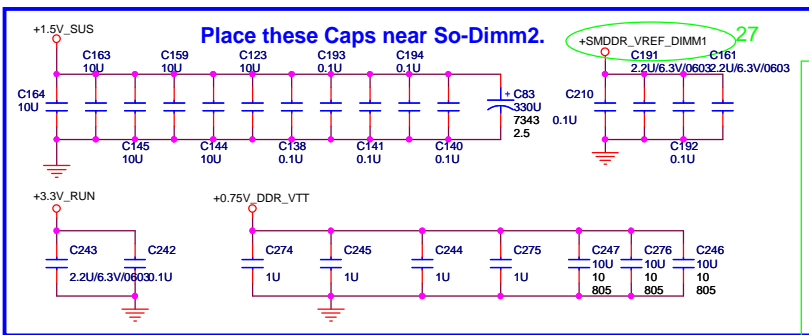
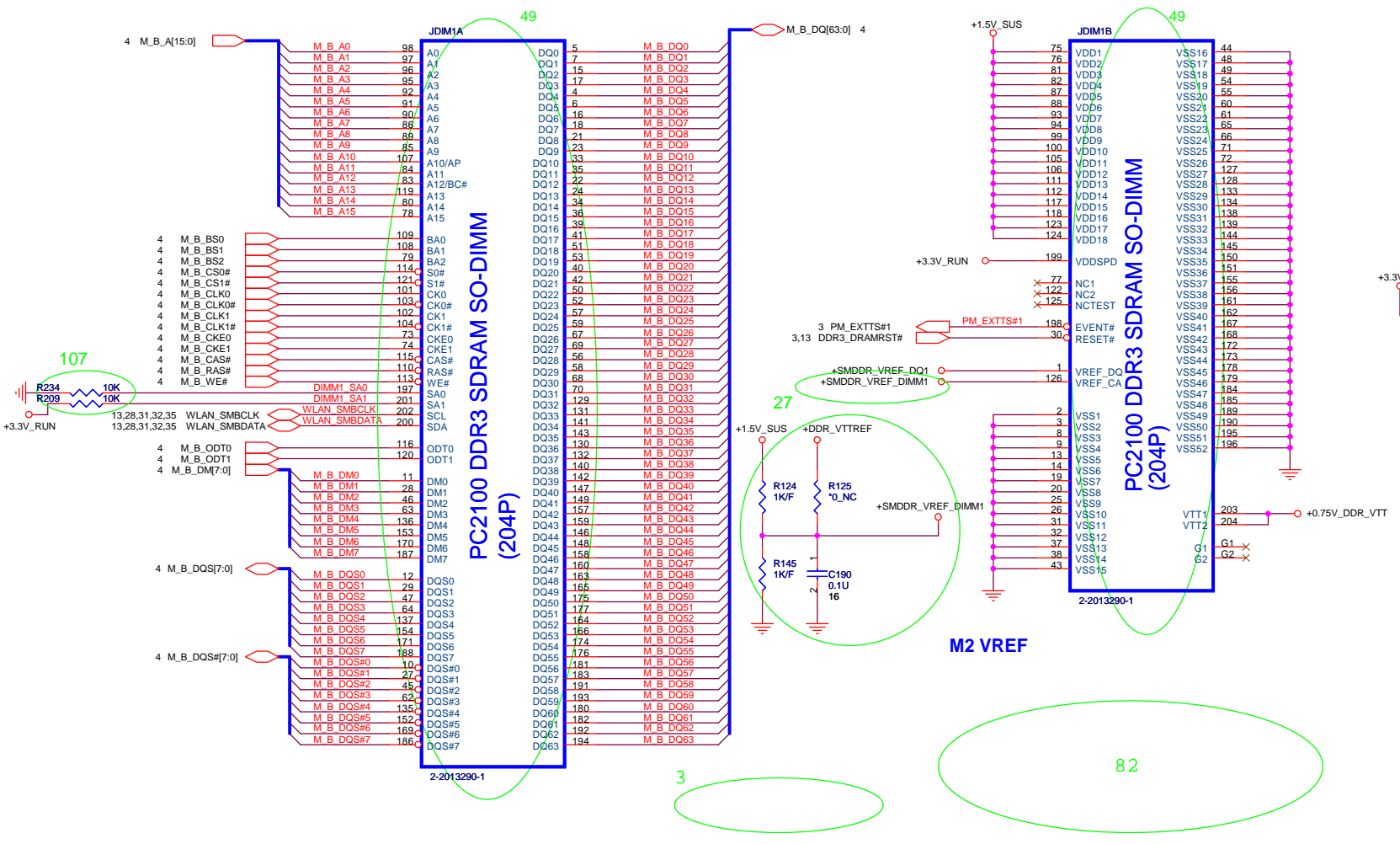
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IBEX PEAK-M (GND)



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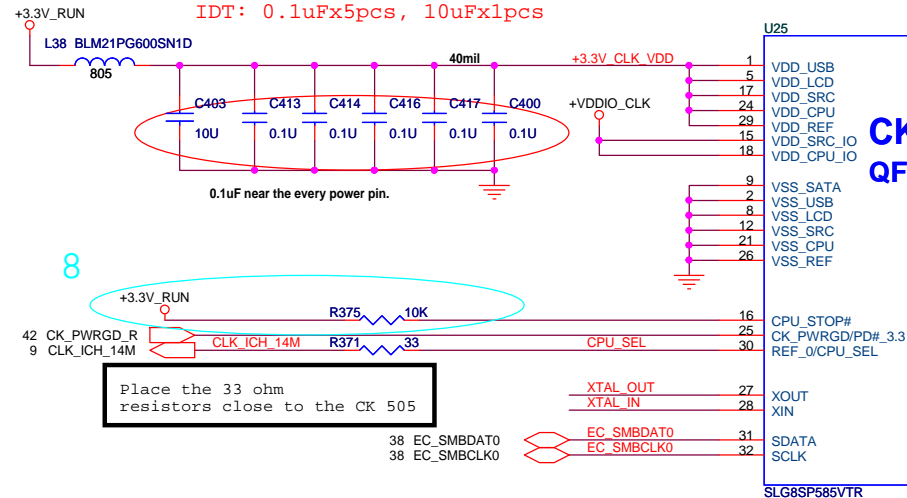




	VREF_DQ	R59	R58	R43
M1	stuff	X	X	(+DDR_VTREF)
M3	X	stuff	X	X

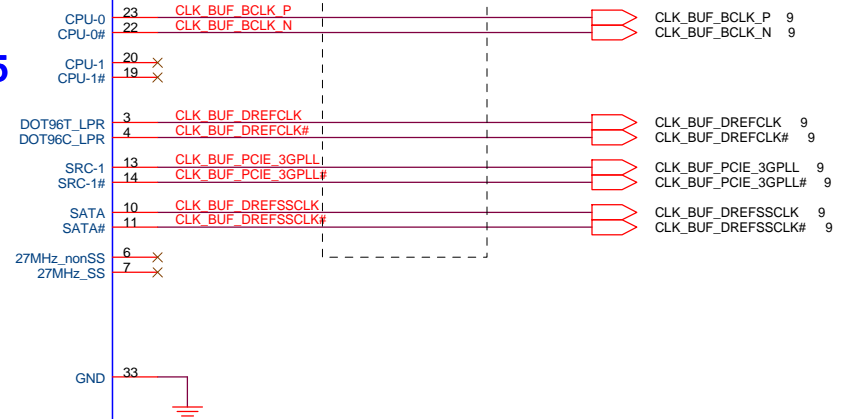


Realtek: 0.1uF x 6 pcs, 22uF x 1 pcs
 IDT: 0.1uF x 5 pcs, 10uF x 1 pcs

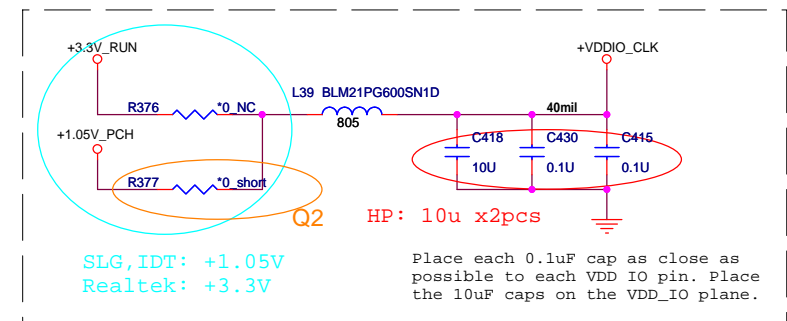
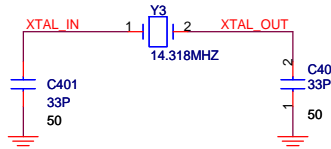
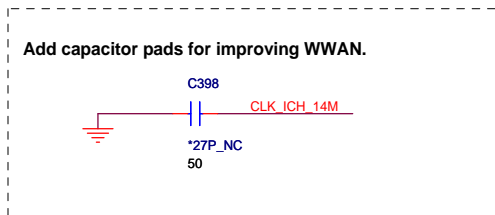


**CK505
QFN32**

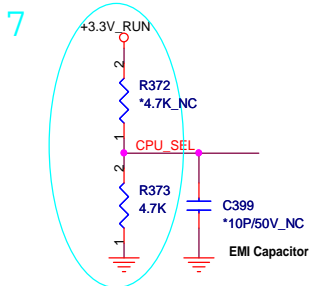
Place within 0.5" of CLKGEN



Realtek: 0.1uF x 3 pcs, 22uF x 1 pcs
 IDT: 0.1uF x 2 pcs, 10uF x 1 pcs




+VDDIO_CLK:
 SLG date sheet (V0.2) P15: Min 1.05V, Max 3.465V.
 Realtek date sheet (V1.2) P11: Min 1.05V, Max 3.3V.
 IDT date sheet (V0.7) P10: Min 0.9975V, Max 3.465V.



PIN	30	CPU_0	CPU_1
0 (default)		133MHz	133MHz
1 (0.7V-1.5V)		100MHz	100MHz

CPU_SEL:
 SLG date sheet (V0.2) P15:
 High Voltage: Min 0.7V, Max 1.5V.
 Low Voltage: Min Vss-0.3V, Max 0.35V.
 Realtek date sheet (V1.2) P11:
 High Voltage: Min 0.7V, Max 1.5V.
 Low Voltage: Min Vss-0.3V, Max 0.35V.
 IDT date sheet (V0.7) P10:
 High Voltage: Min 0.7V, Max 1.5V.
 Low Voltage: Min Vss-0.3V, Max 0.35V.


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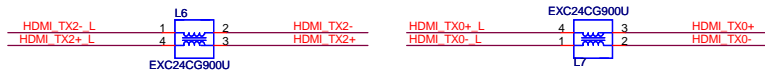
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		QUANTA COMPUTER	
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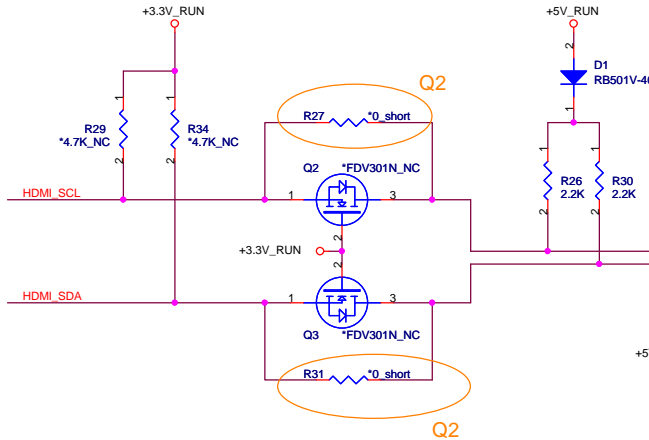
**BLANK PAGE FOR PAGE
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 QUANTA COMPUTER		
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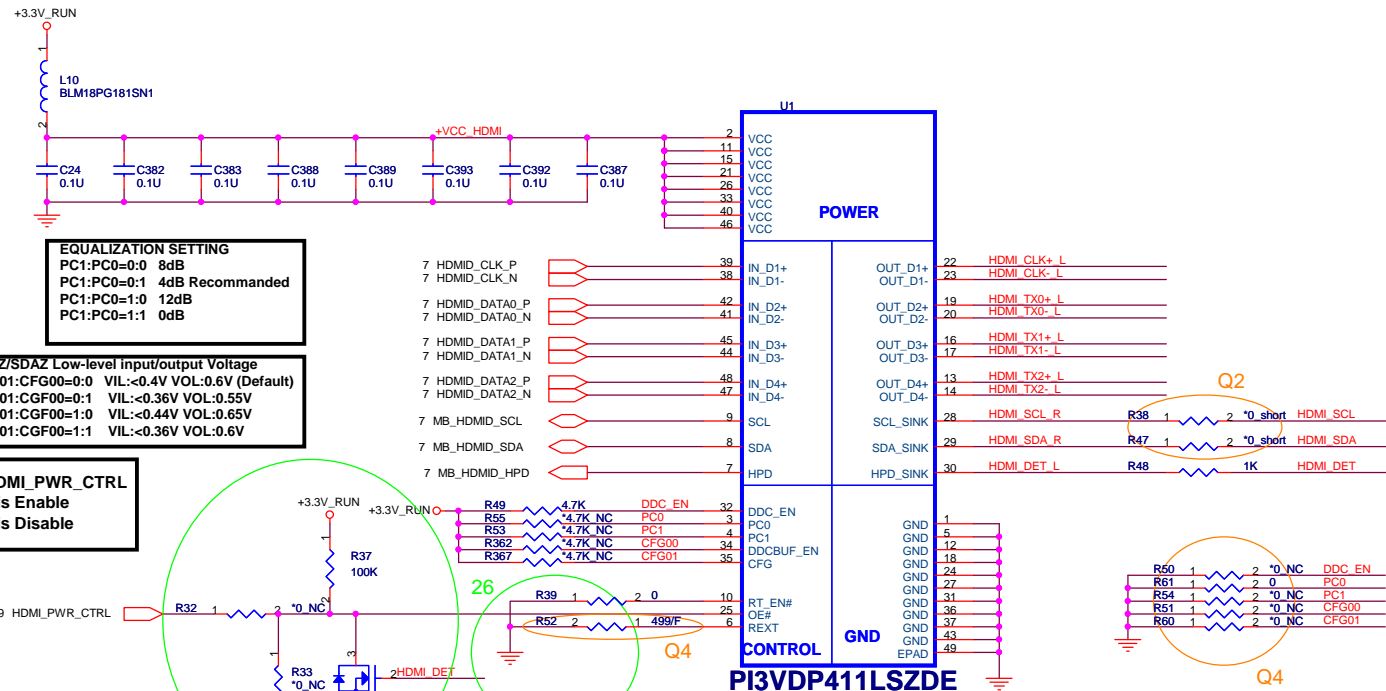
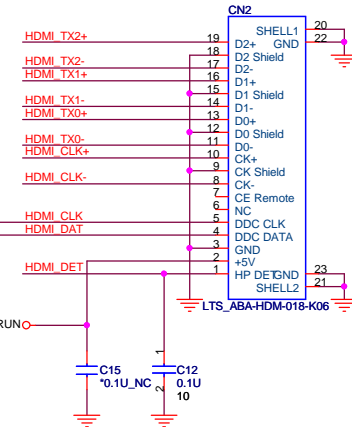


Reserve for EMI and close to HDMI CONN

HDMI_CLK+ L	R7	300	HDMI_CLK C	C16	0.1U	HDMI_CLK- L
HDMI_TX0+ L	R8	300	HDMI_TX0 C	C19	0.1U	HDMI_TX0- L
HDMI_TX1+ L	R15	300	HDMI_TX1 C	C20	0.1U	HDMI_TX1- L
HDMI_TX2+ L	R16	300	HDMI_TX2 C	C22	0.1U	HDMI_TX2- L

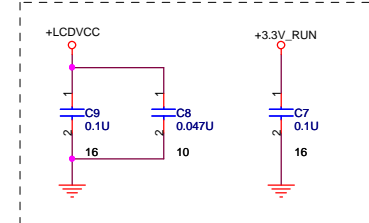
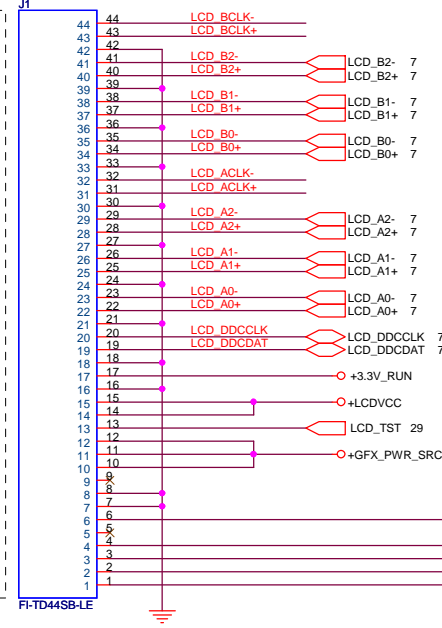
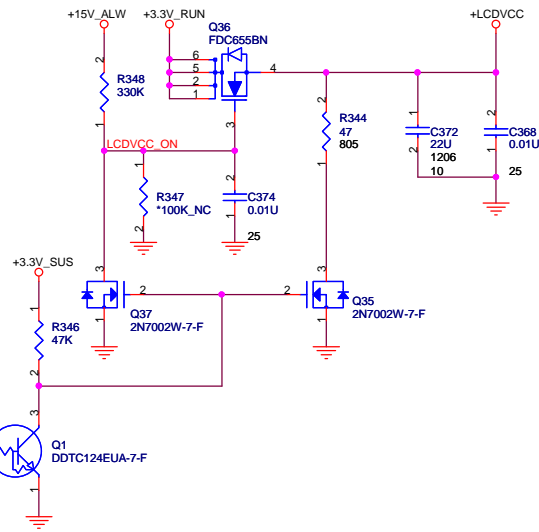
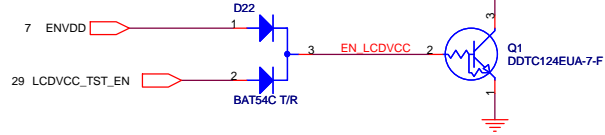


HDMI

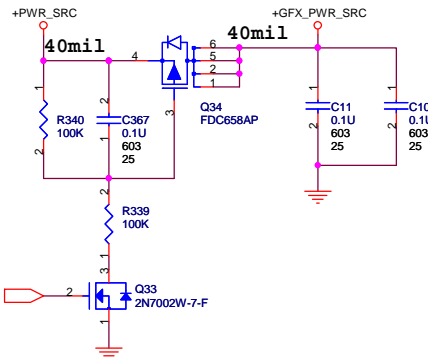
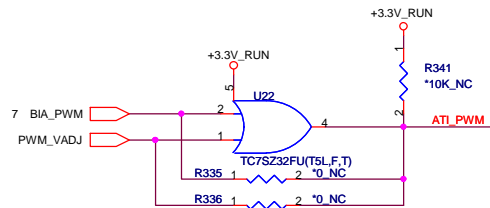


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Support the new imbedded diagnostics.

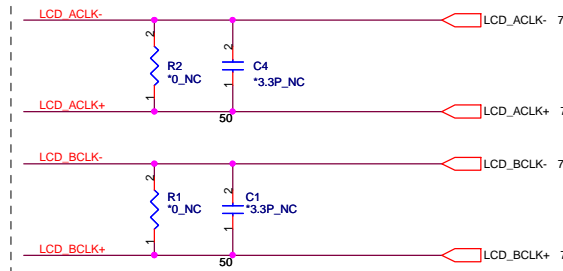


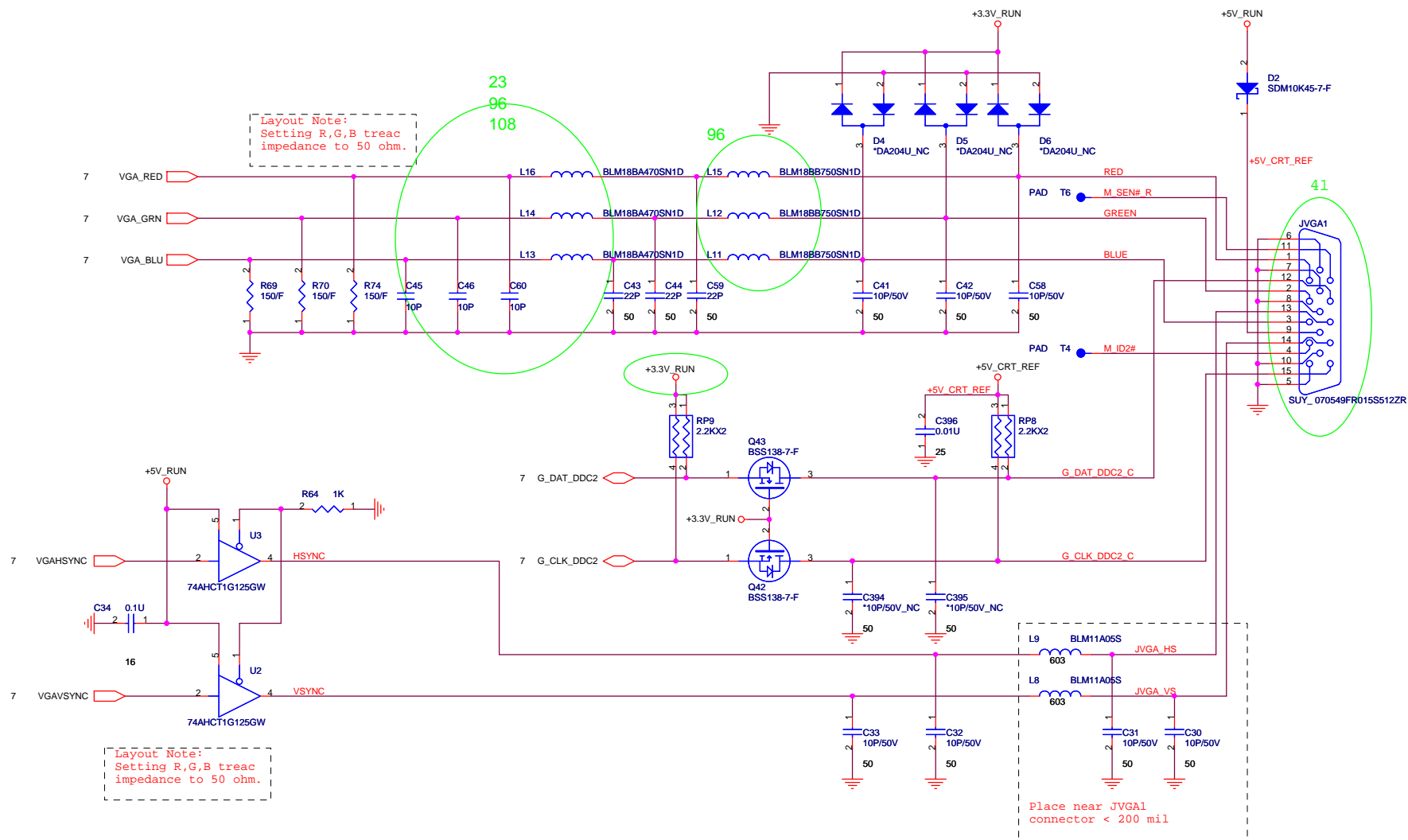
Address : A9H --Contrast
AAH --Backlight

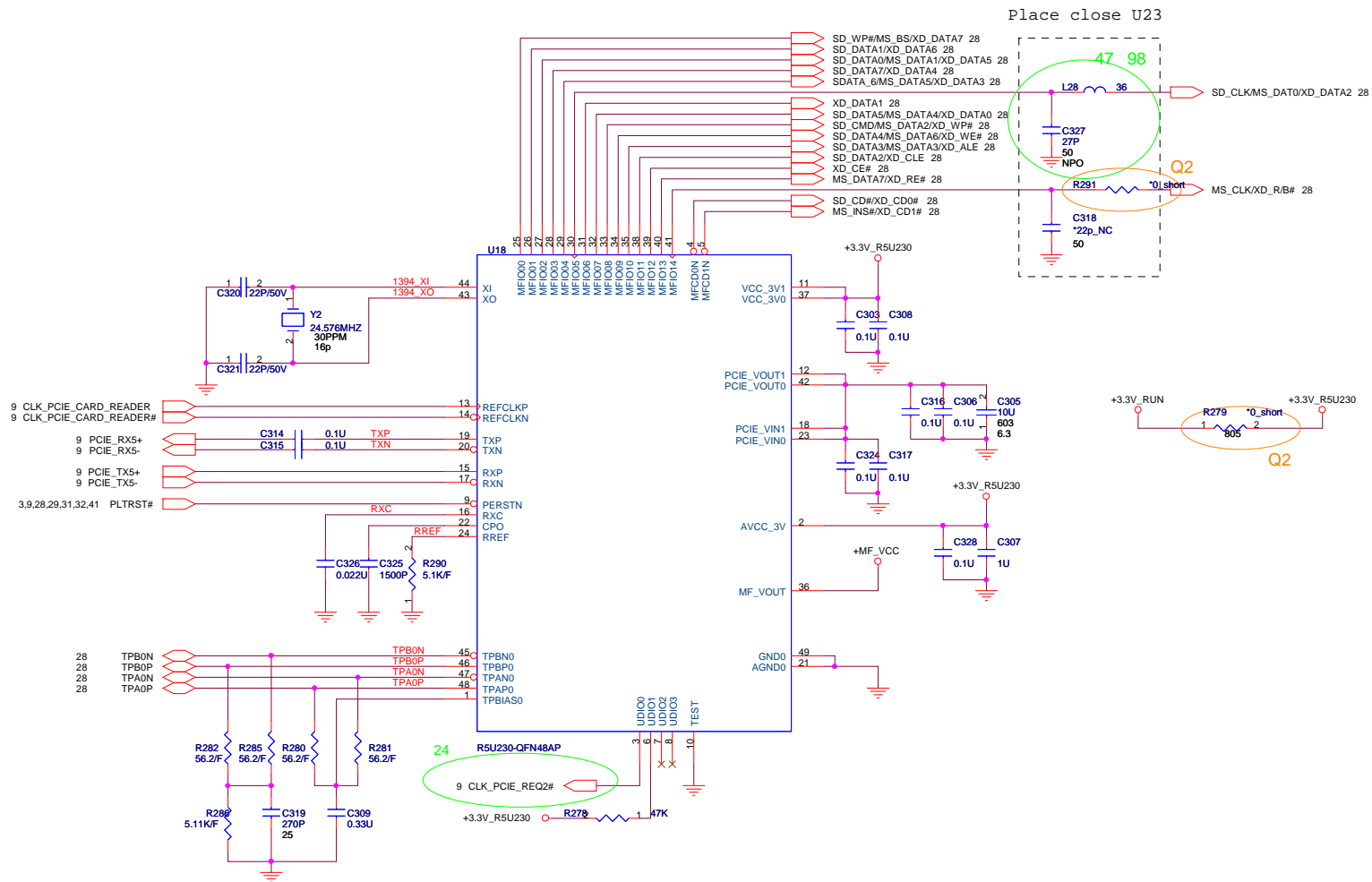


Shunt capacitors on LVDS for improving WWAN.

LCD_B0-	C13	1	2	*3.3P_NC	50	LCD_B0+
LCD_B1-	C3	1	2	*3.3P_NC	50	LCD_B1+
LCD_B2-	C2	1	2	*3.3P_NC	50	LCD_B2+
LCD_A0-	C6	1	2	*3.3P_NC	50	LCD_A0+
LCD_A1-	C5	1	2	*3.3P_NC	50	LCD_A1+
LCD_A2-	C14	1	2	*3.3P_NC	50	LCD_A2+







MFIO Pin Assignment Table

MFIO	SD8	MS8	XD
00	WP	BS	D7
01	D1	-	D6
02	D0	D1	D5
03	D7	-	D4
04	D6	D5	D3
05	CLK	D0	D2
06	-	-	D1
07	D5	D4	D0
08	CMD	D2	WP#
09	D4	D6	WE#
10	D3	D3	ALE
11	D2	-	CLE
12	-	-	CE#
13	-	D7	RE#
14	-	CLK	R/B#

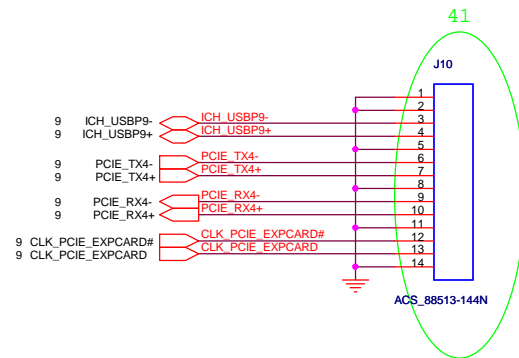
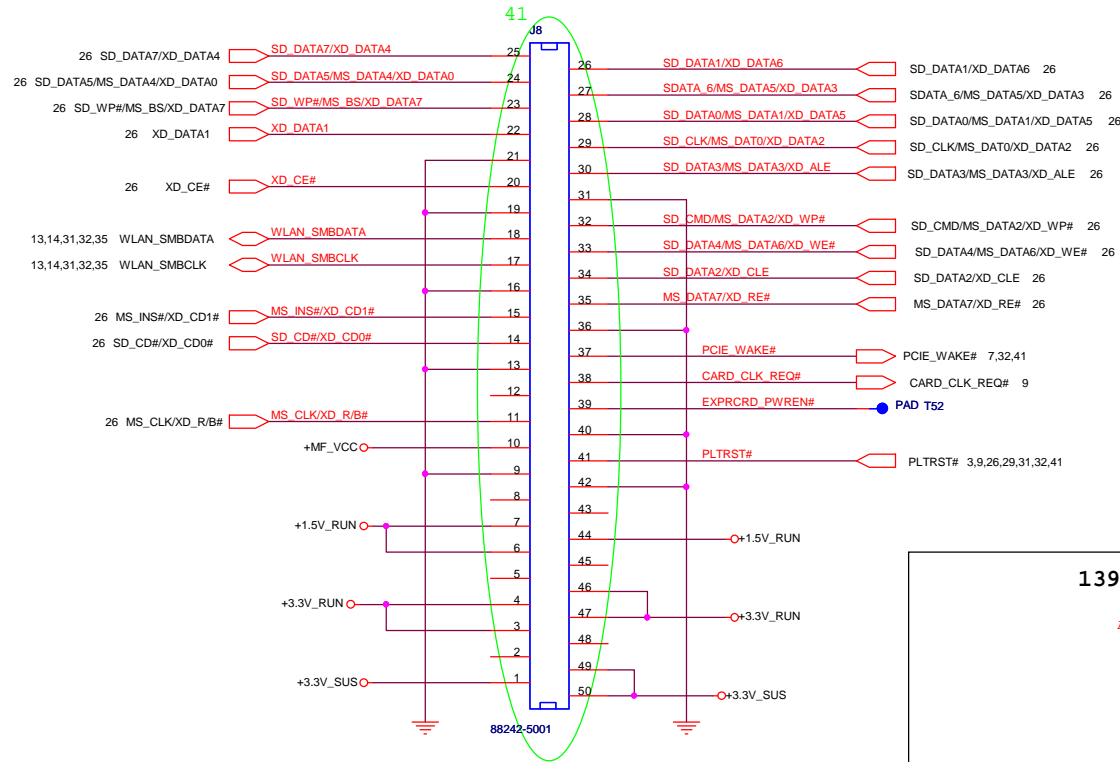


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COMPUTER

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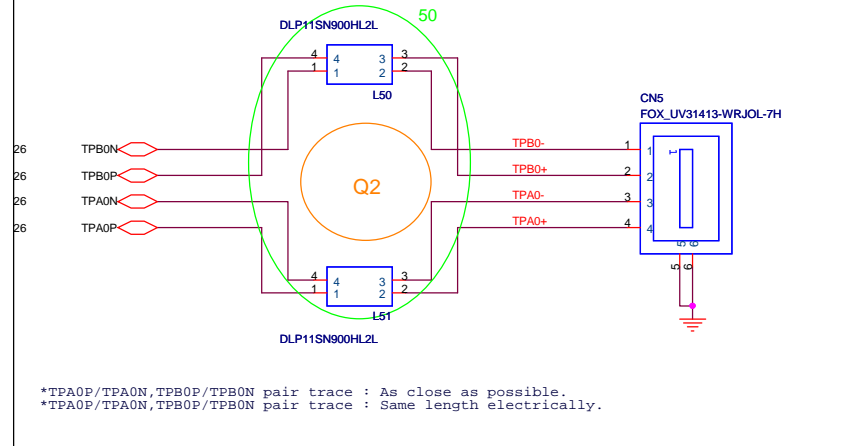
**BLANK PAGE FOR PAGE
NUMBER SAME AS DISCRETE**

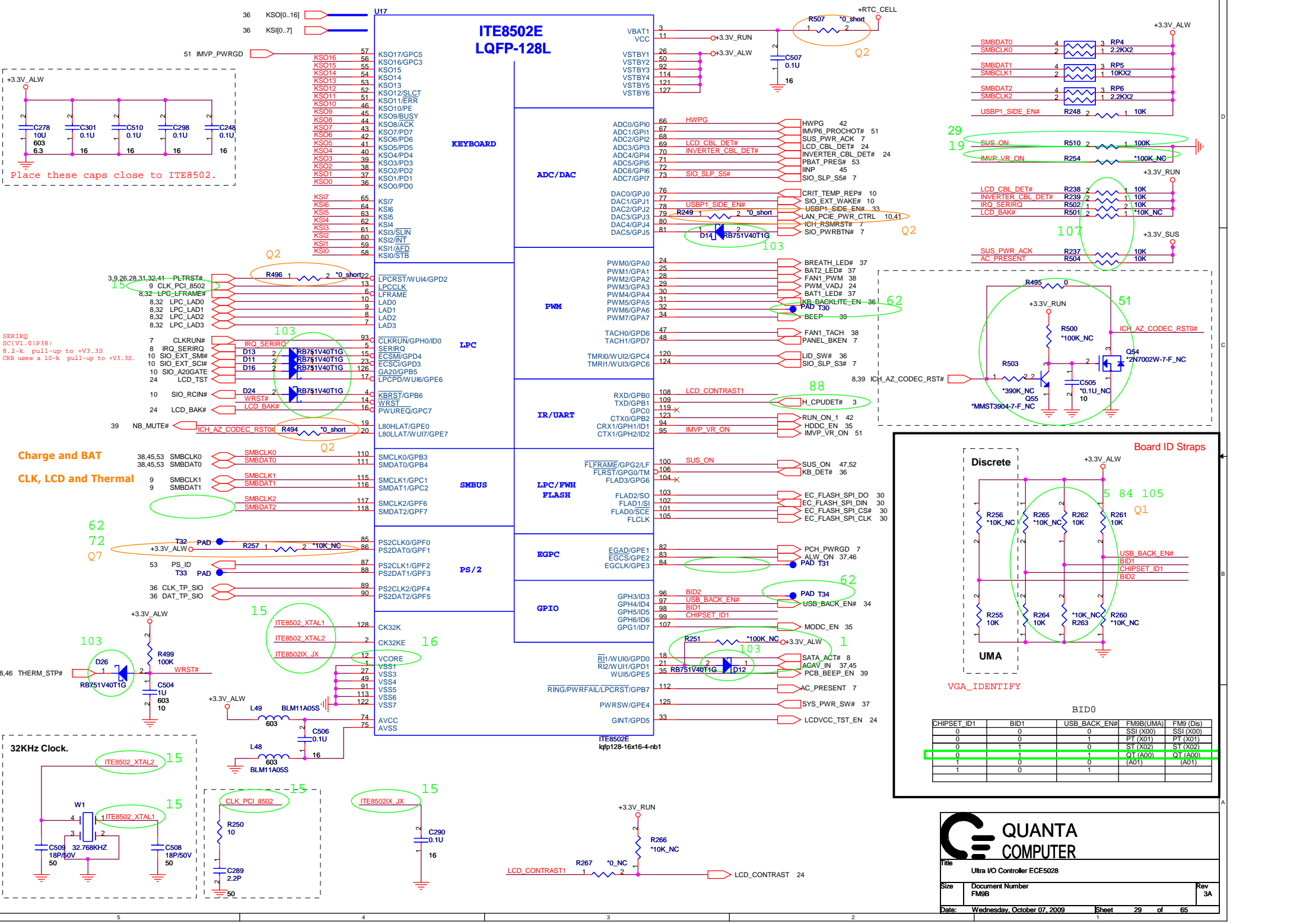
Express Card/CARD READER



1394 CONNECTOR

AS CLOSE AS POSSIBLE TO 1394 CONNECTOR.

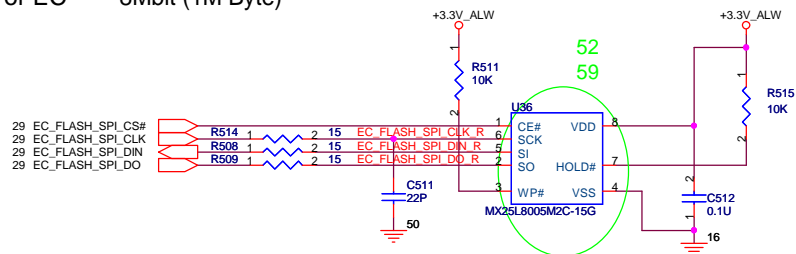




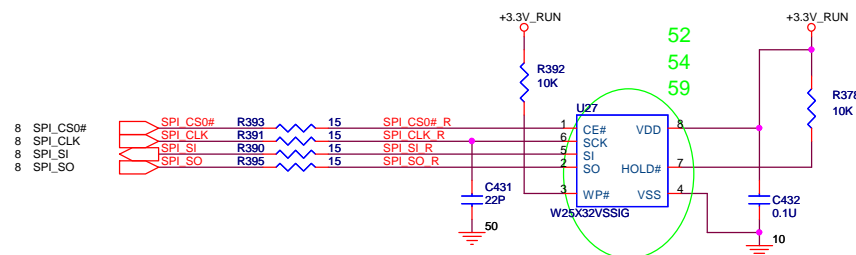
BID0				
CHIPSET ID1	BID1	USB BACK EN#	FM9B(UMA)	FM9(Ds)
0	0	0	SSI (X00)	SSI (X00)
0	0	1	PT (X01)	PT (X01)
0	1	0	ST (X02)	ST (X02)
0	1	1	QT (A00)	QT (A00)
1	0	0	(A01)	(A01)
1	0	1		



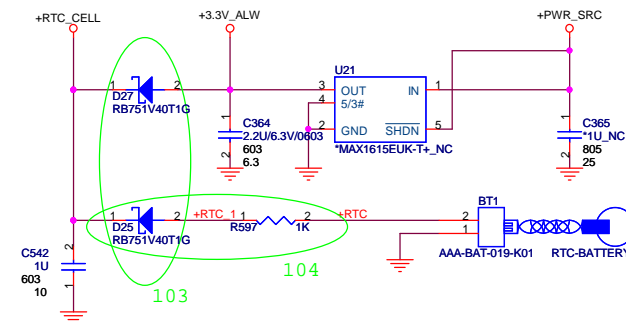
For EC 8Mbit (1M Byte)



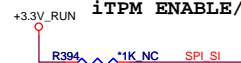
For PCH 32Mbit (4M Byte)



RTC BATTERY



iTPM ENABLE/DISABLE



TPM Function	R712
Enable	Mount
Disable	NC (Default)



Ultra I/O Controller ECE5028

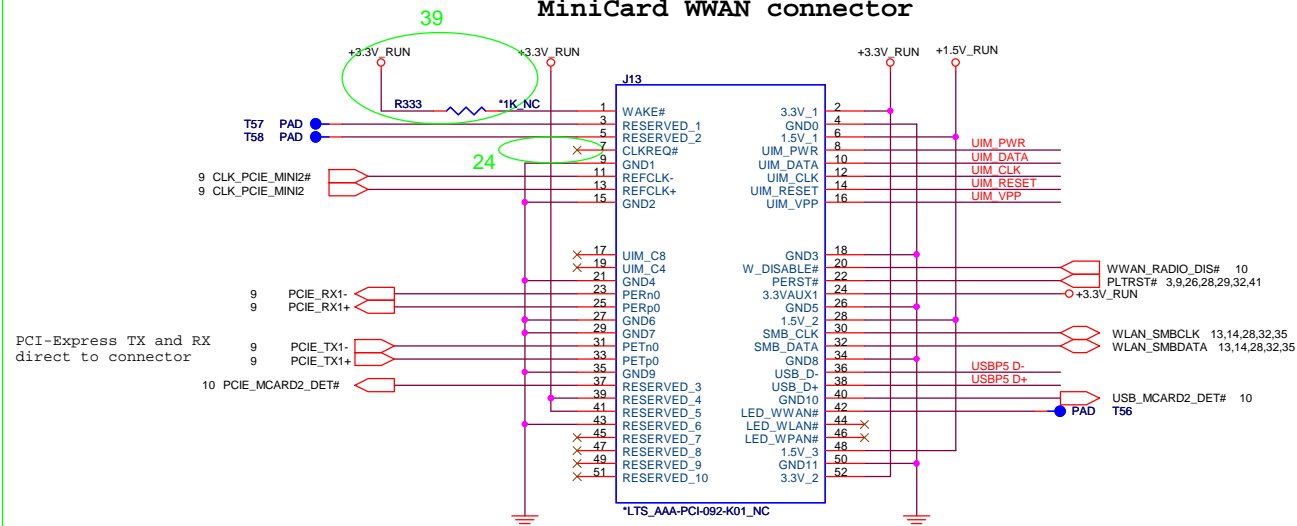
Size Document Number FM9B

Date: Thursday, October 01, 2009

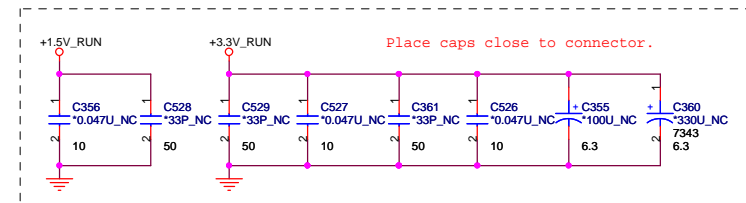
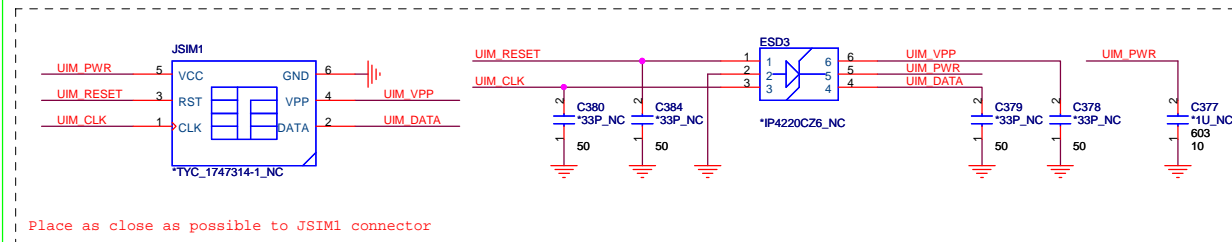
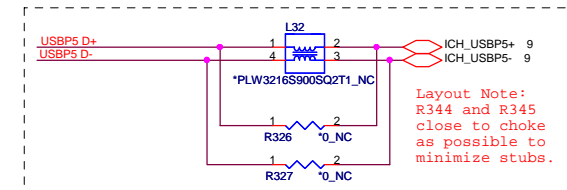
Sheet 30 of 65

Rev 3A

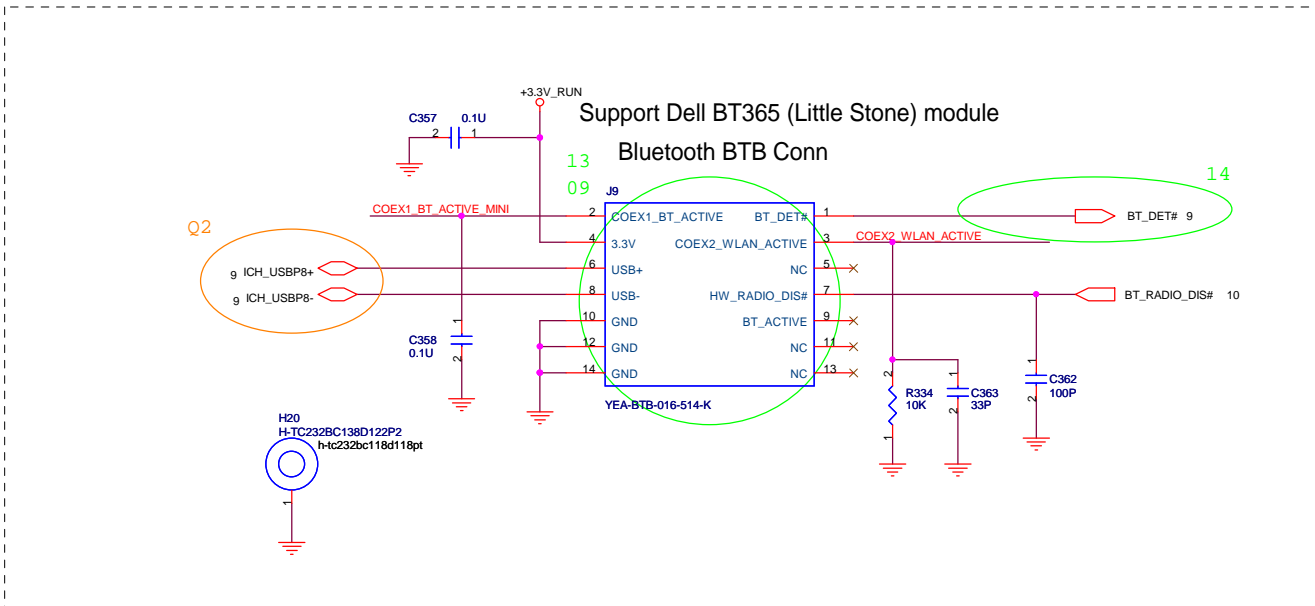
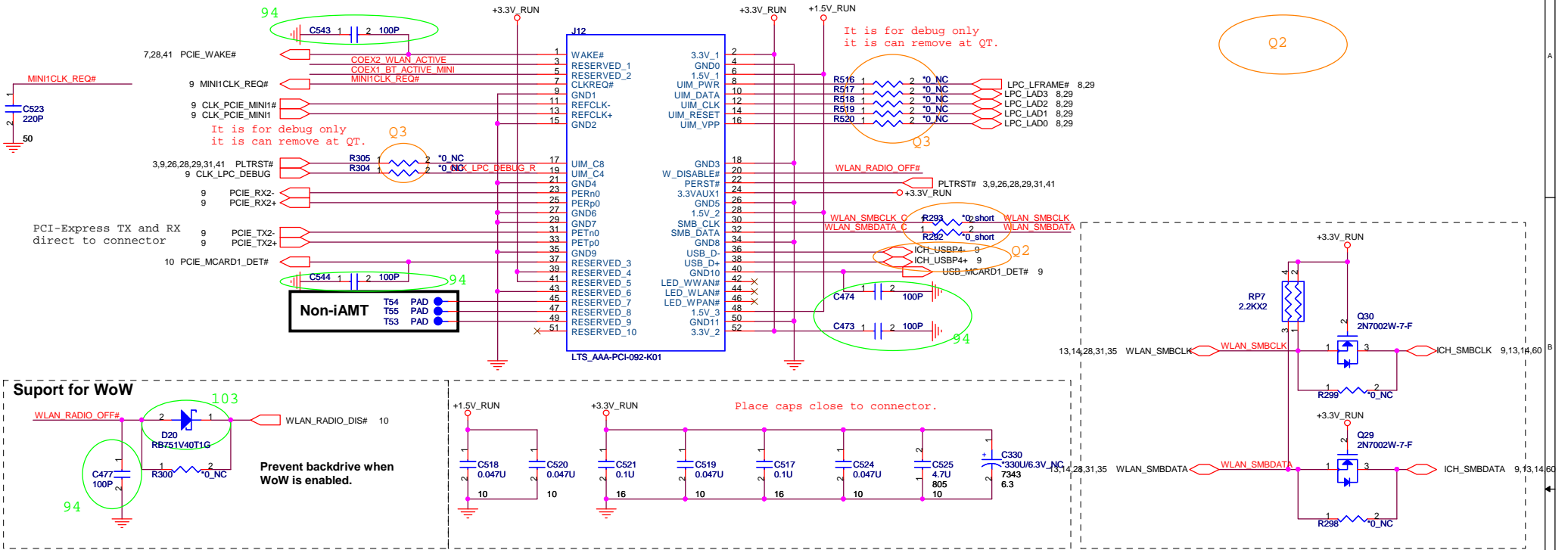
MiniCard WWAN connector



PCI-Express TX and RX
direct to connector



MiniCard WLAN connector



Title

MDC CONN.

Size

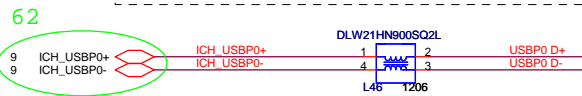
Document Number

Rev

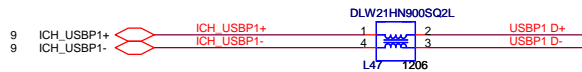
Date: Friday, October 02, 2009

Sheet 32 of 65

External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently



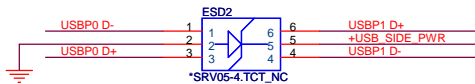
Q2



Q2

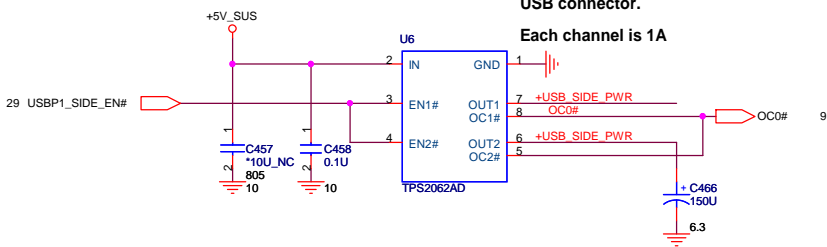
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

Place ESD diodes as close as USB connector.



Place one 150uF cap by each USB connector.

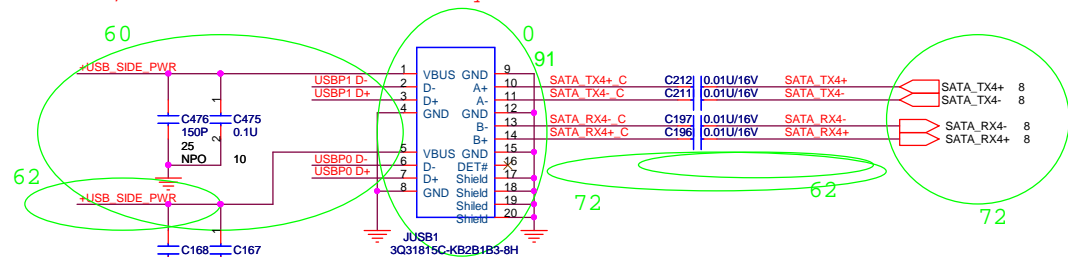
Each channel is 1A



62

Side External USBX2

PN is old, Because New Part can't ready before SST build.



Please put those on the same side of MB PCB

USBx2 & ESATA COMBO

USB BUS SW

62

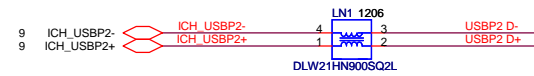
E-SATA Re-driver

72

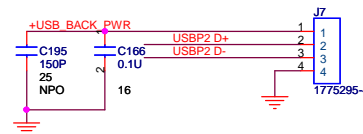
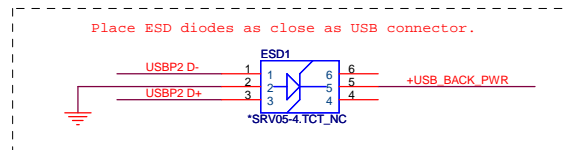
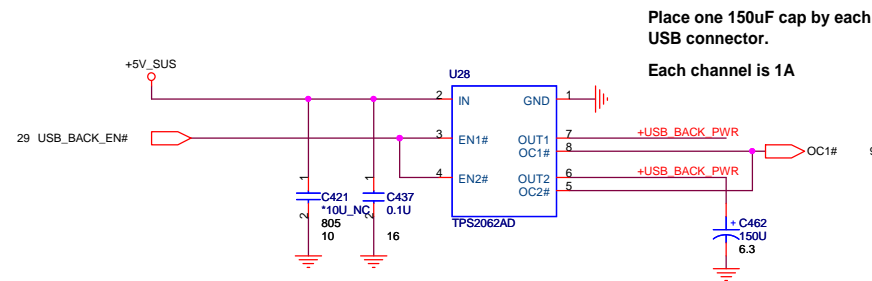
62



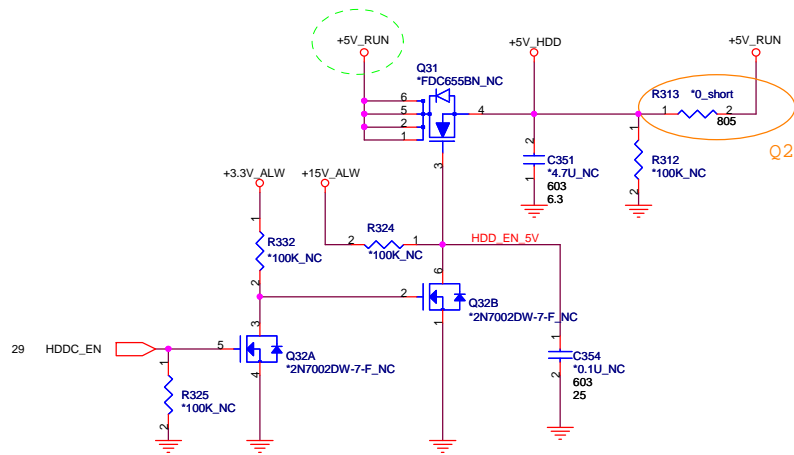
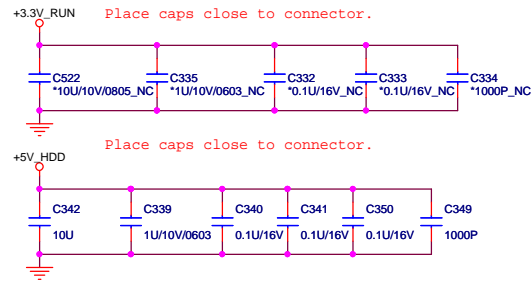
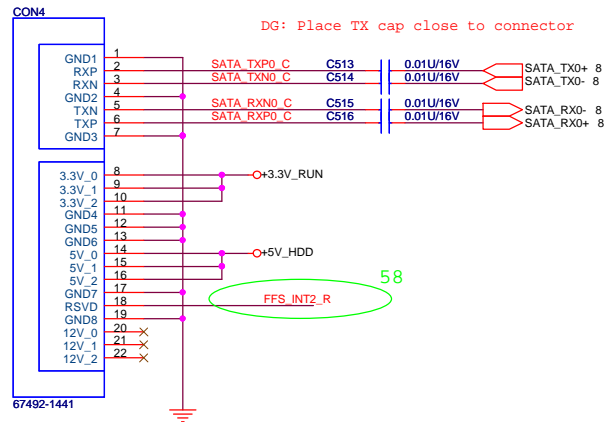
Title		
SERIAL PORT & USB		
Size	Document Number	Rev
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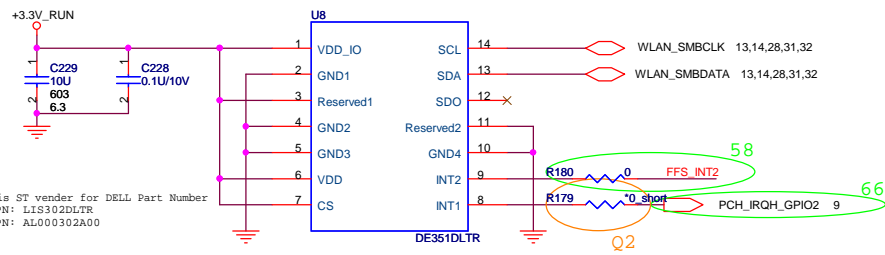
Q2



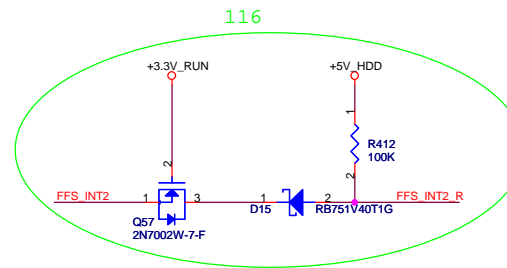
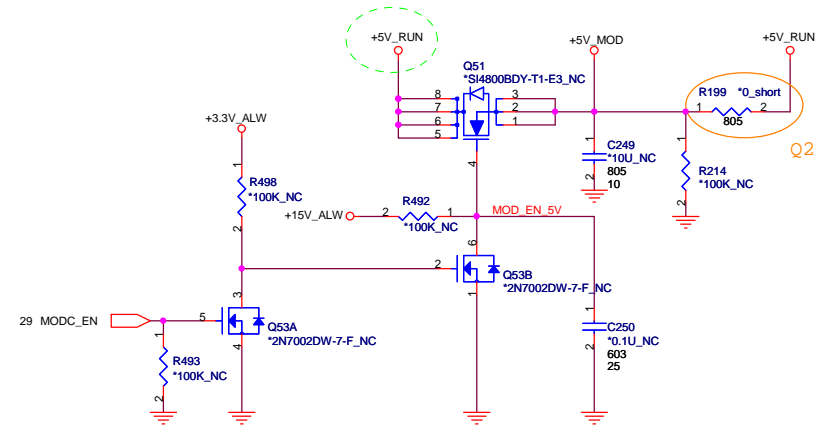
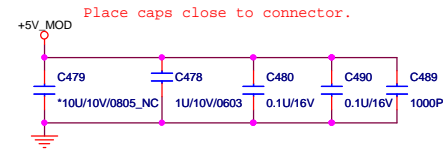
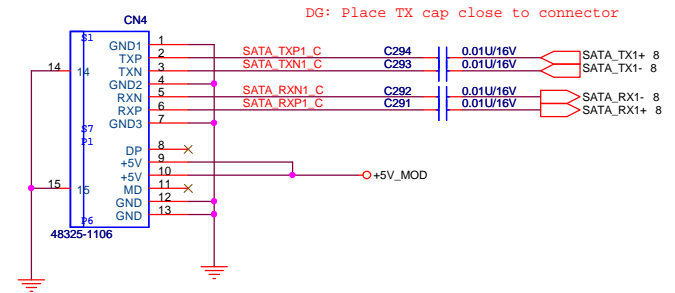
SATA Connector.



3-axis Fall Sensor (HDD data protector)



ODD Connector

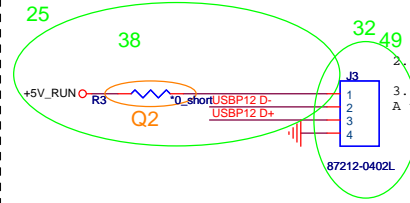


Title			SATA (HDD&CD_ROM)
Size	Document Number	Rev	
	FM9B	3A	
Date:	Monday, October 05, 2009	Sheet	35 of 65

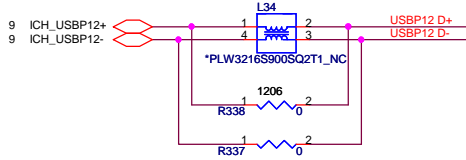
of 65

Touch Screen Module

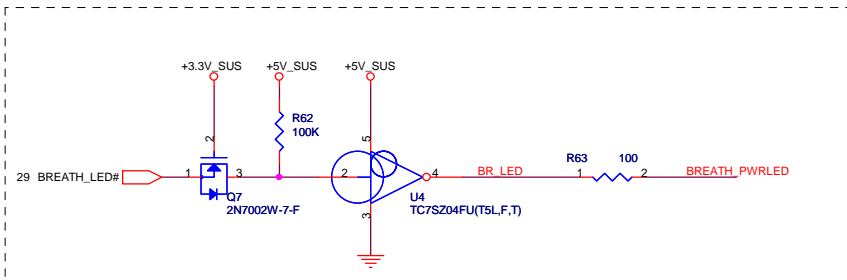
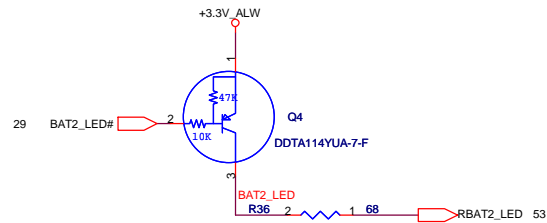
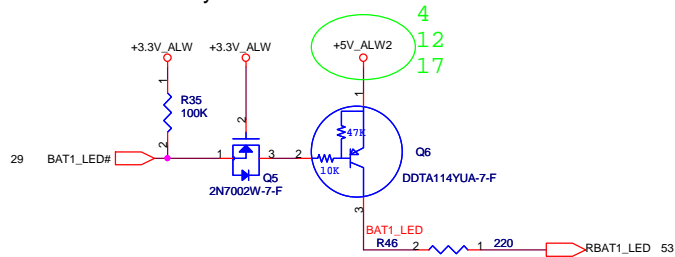
- Note:
1. VBUS IND:VBUS indication should be supplied to single the DuoSense to connect According to the USB 2.0 specification. A GND voltage from the host should indicate a connection.
 2. Maximum cable resistance on VCC, GND should be 150m ohm.
 3. FPC cable should support 12MHz USB singles. A tri-state should indicate no connection.



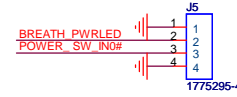
Need check the connector footprint and symbol.



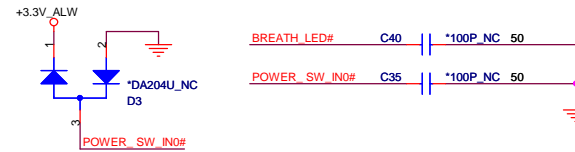
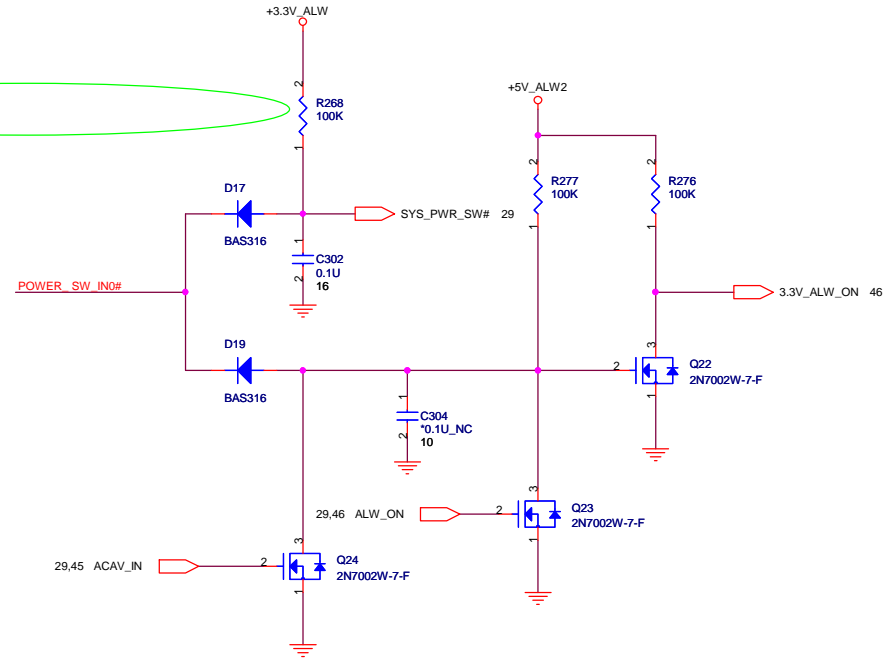
Battery status.



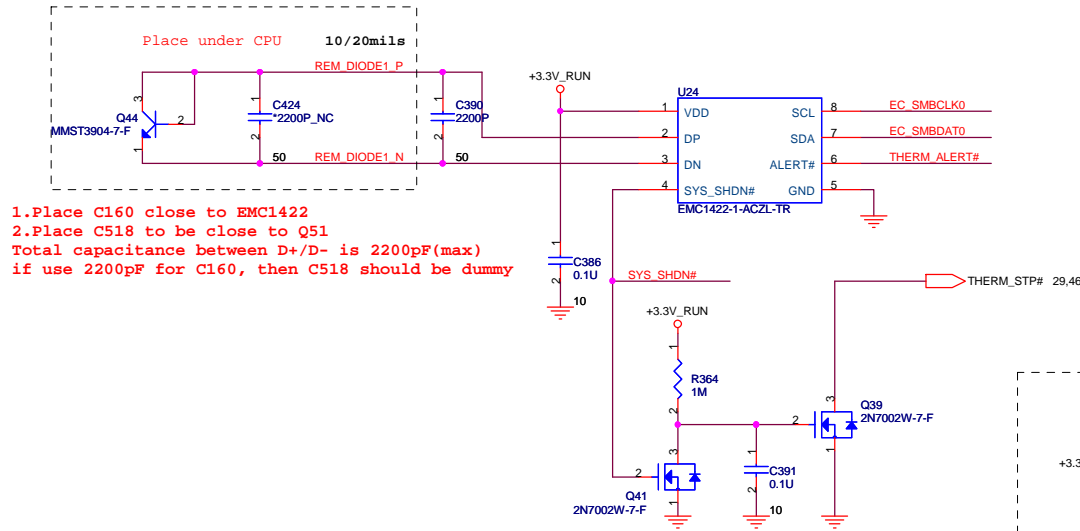
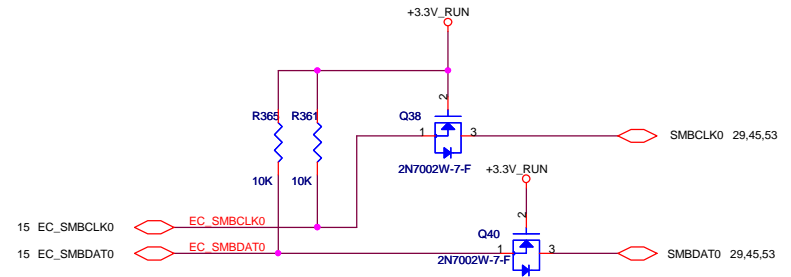
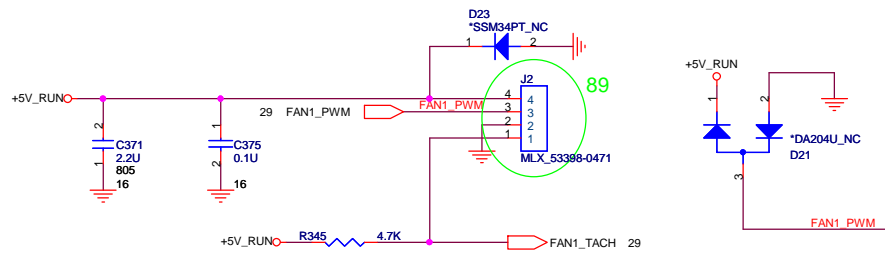
Power button Cable



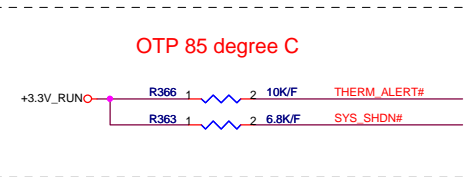
3VALW ON POWER LOGIC

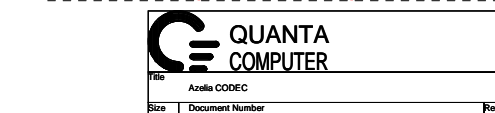
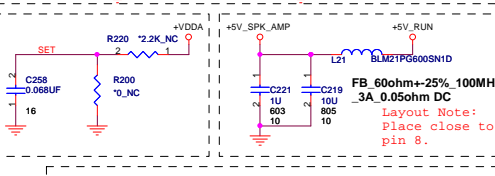
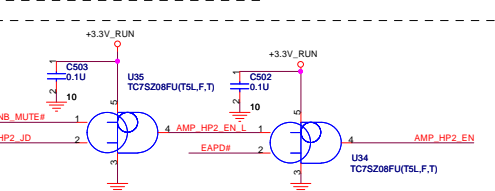
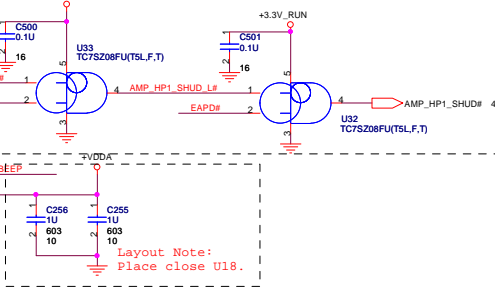
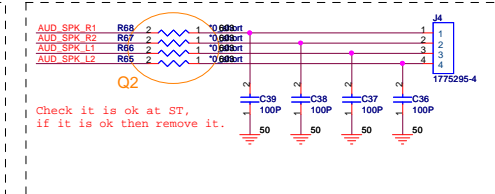


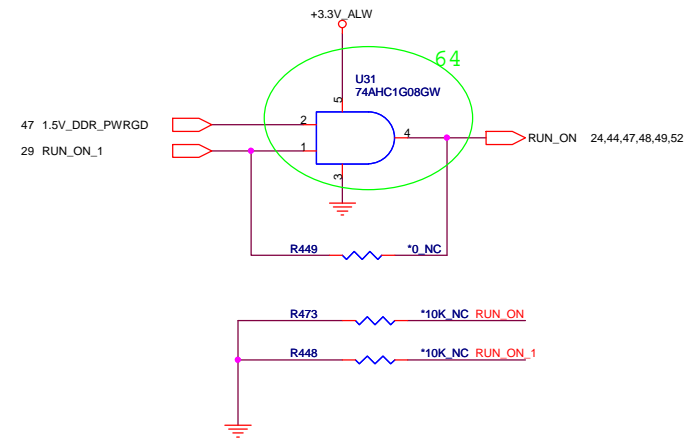
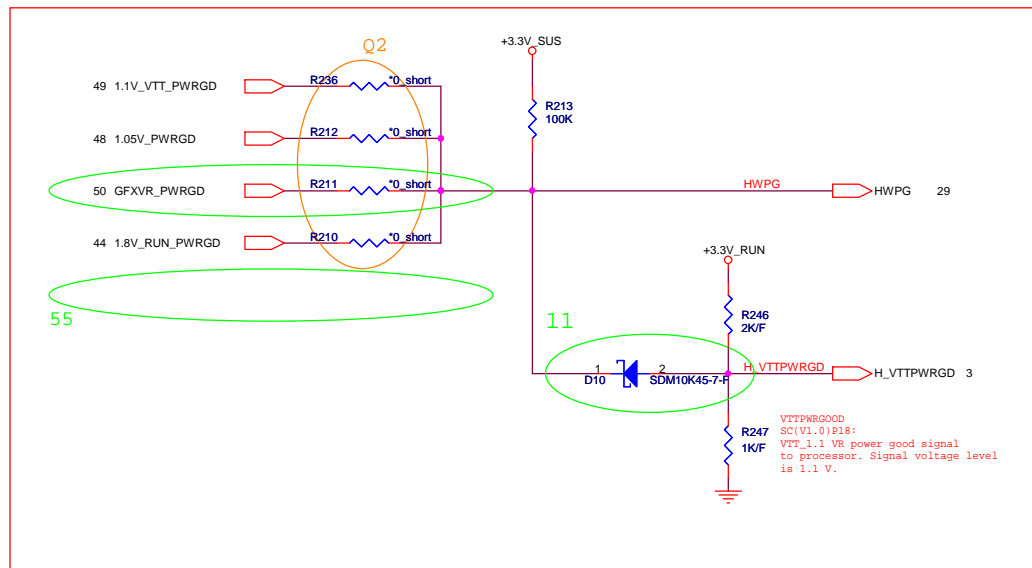
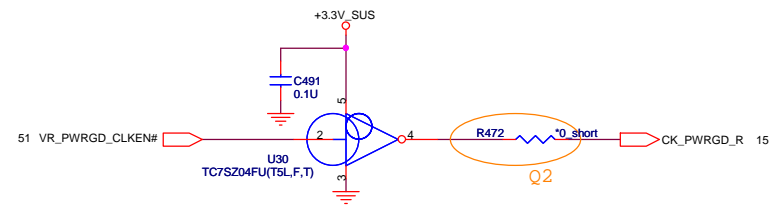
Title		
SWITCH, KEYBOARD & LED&Touch Screen Module		
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- 1.Place C160 close to EMC1422
 - 2.Place C518 to be close to Q51
- Total capacitance between D+/D- is 2200pF(max)
if use 2200pF for C160, then C518 should be dummy

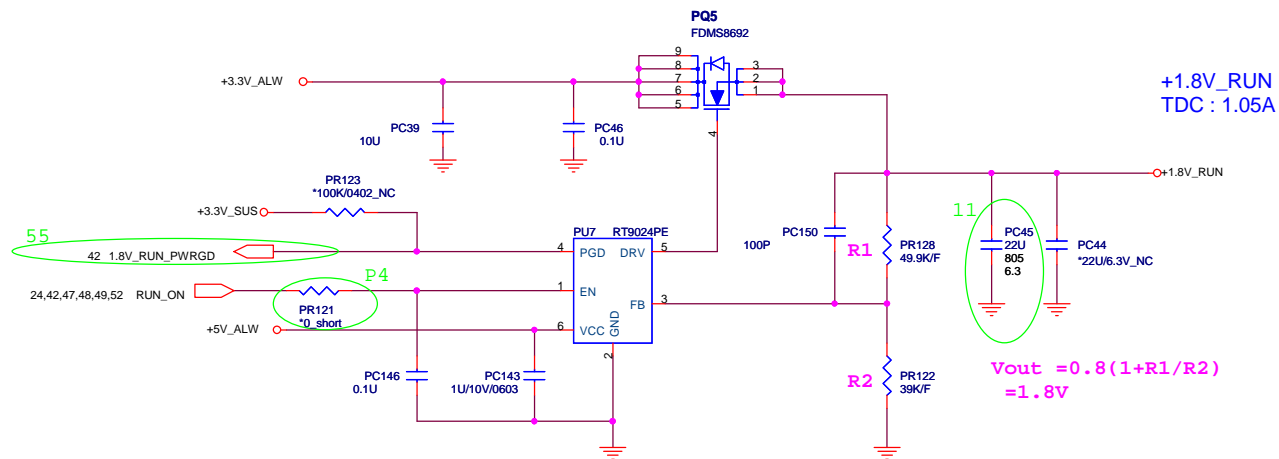






	1	2	3	4	5
A					
B					
C					
D					
	1	2	3	4	5

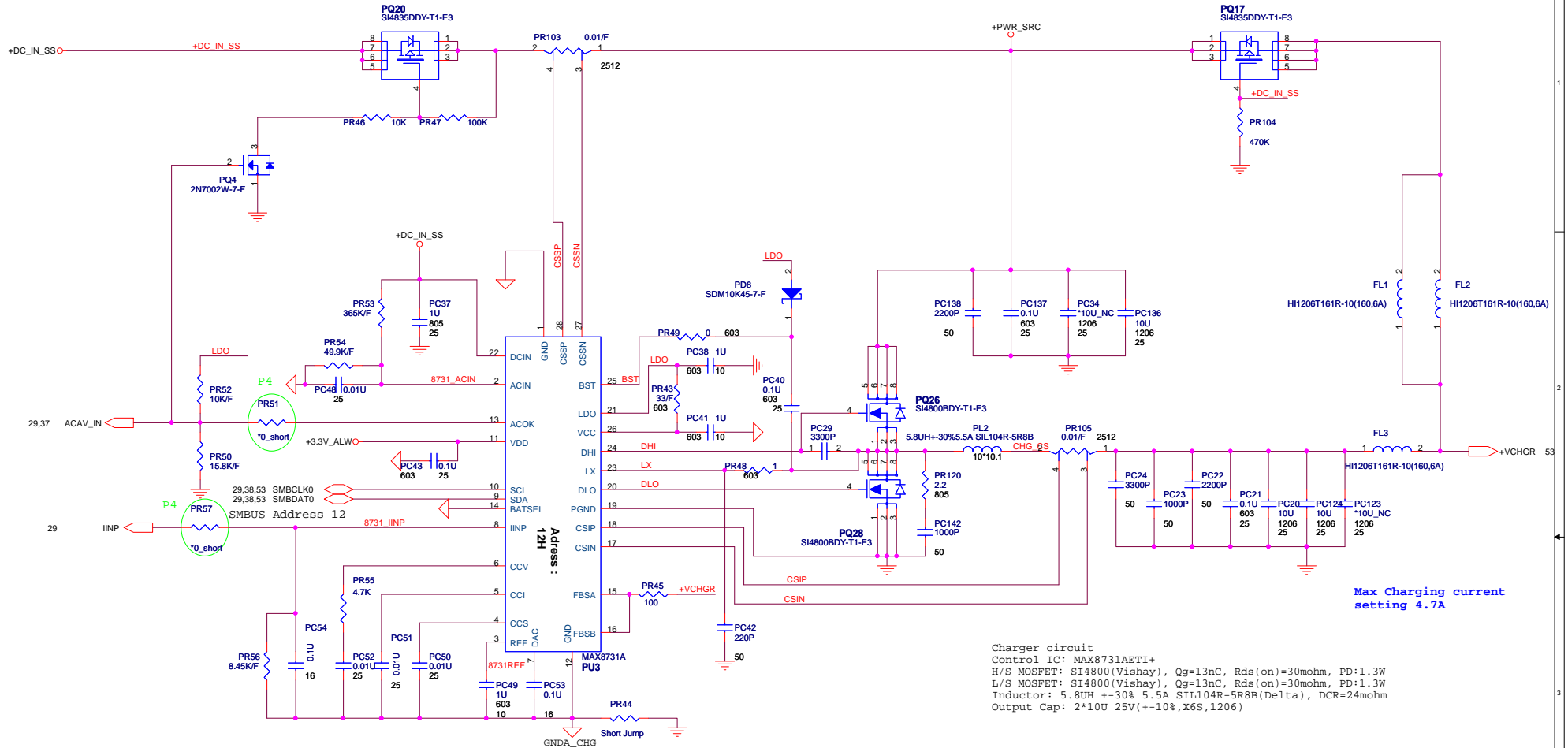
 <div>QUANTA COMPUTER</div>		
Title Battery Selector		
Size	Document Number FM9B	Rev 3A
Date: Thursday, October 01, 2009	Sheet 43 of 65	



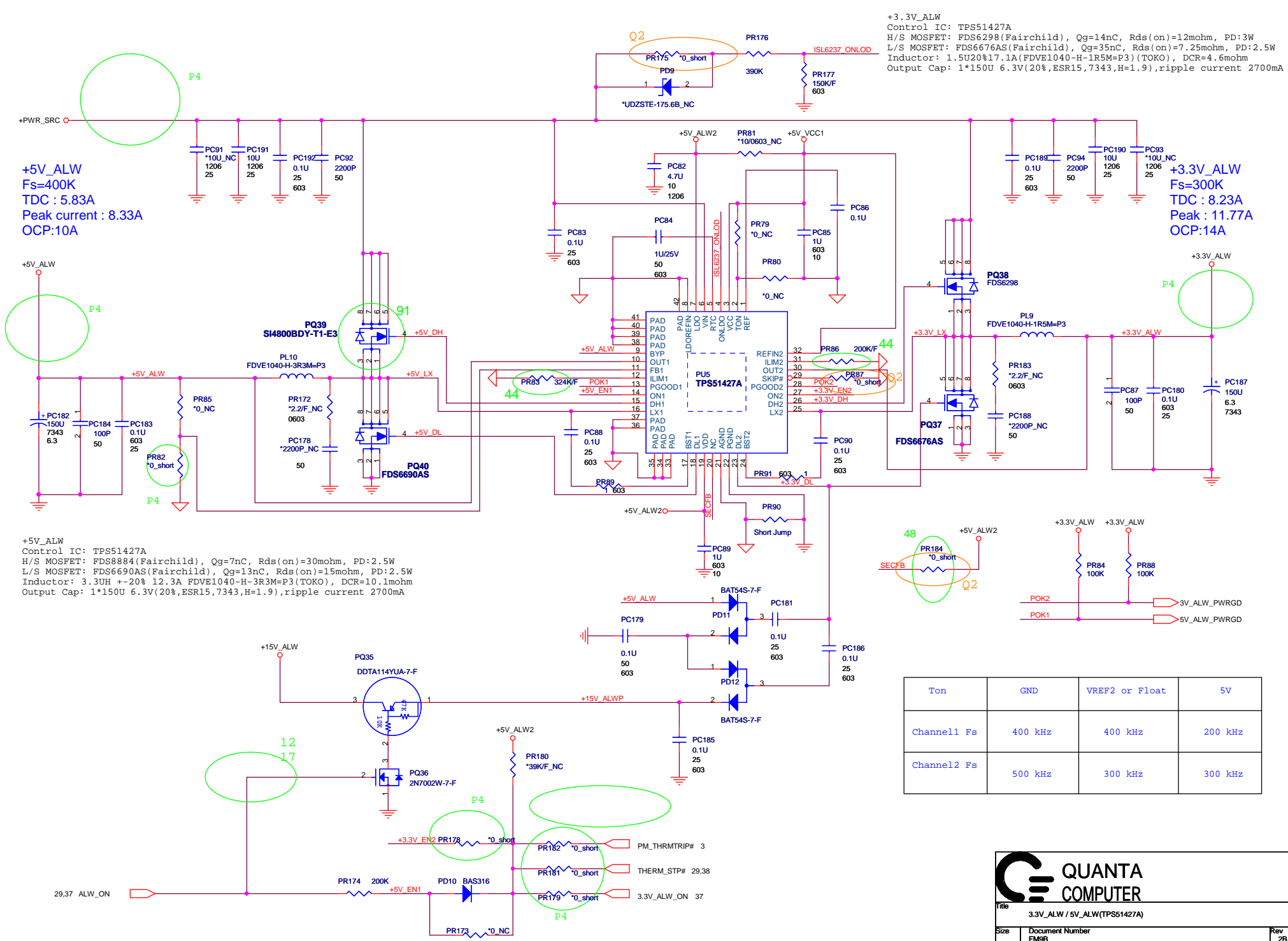
Title		
+1.8V_RUN(RT9024)		
Size	Document Number	Rev
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Continuous current : 13A
Rds(on) : 18mohm

Continuous current : 13A
Rds(on) : 18mohm



Title			
Charger (MAX8731)			
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+3.3V_ALW
Control IC: TPS51427A
H/S MOSFET: FDS6298(Fairchild), Qg=14nC, Rds(on)=12mohm, PD:3W
L/S MOSFET: FDS6676AS(Fairchild), Qg=35nC, Rds(on)=7.25mohm, PD:2.5W
Inductor: 1.5U20*17.1A(FDVE1040-H-1R5M=P3)(TOKO), DCR=4.6mohm
Output Cap: 1*150U 6.3V(20%,ESR15,7343,H=1.9),ripple current 2700mA

+5V_ALW
Fs=400K
TDC : 5.83A
Peak current : 8.33A
OCP:10A

+3.3V_ALW
Fs=300K
TDC : 8.23A
Peak : 11.77A
OCP:14A

+5V_ALW
Control IC: TPS51427A
H/S MOSFET: FDS8884(Fairchild), Qg=7nC, Rds(on)=30mohm, PD:2.5W
L/S MOSFET: FDS6690AS(Fairchild), Qg=13nC, Rds(on)=15mohm, PD:2.5W
Inductor: 3.3UH +/-20% 12.3A FDVE1040-H-3R3M=P3(TOKO), DCR=10.1mohm
Output Cap: 1*150U 6.3V(20%,ESR15,7343,H=1.9),ripple current 2700mA

Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	400 kHz	200 kHz
Channel2 Fs	500 kHz	300 kHz	300 kHz



QUANTA
COMPUTER

Title

3.3V_ALW / 5V_ALW(TPS51427A)

Size

Document Number

FM9B

Rev

2B

Date:

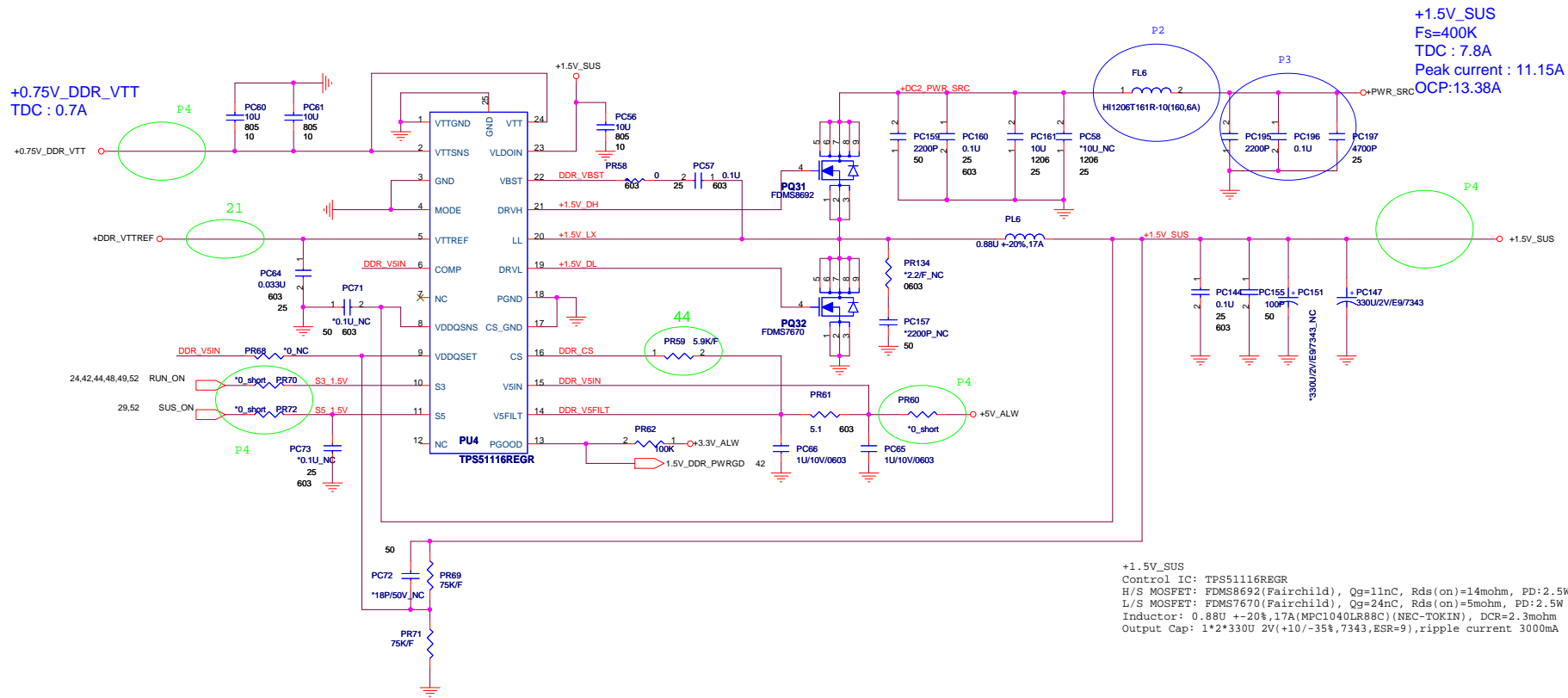
Monday, October 05, 2009

Sheet

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VDDQ and VTT discharge control

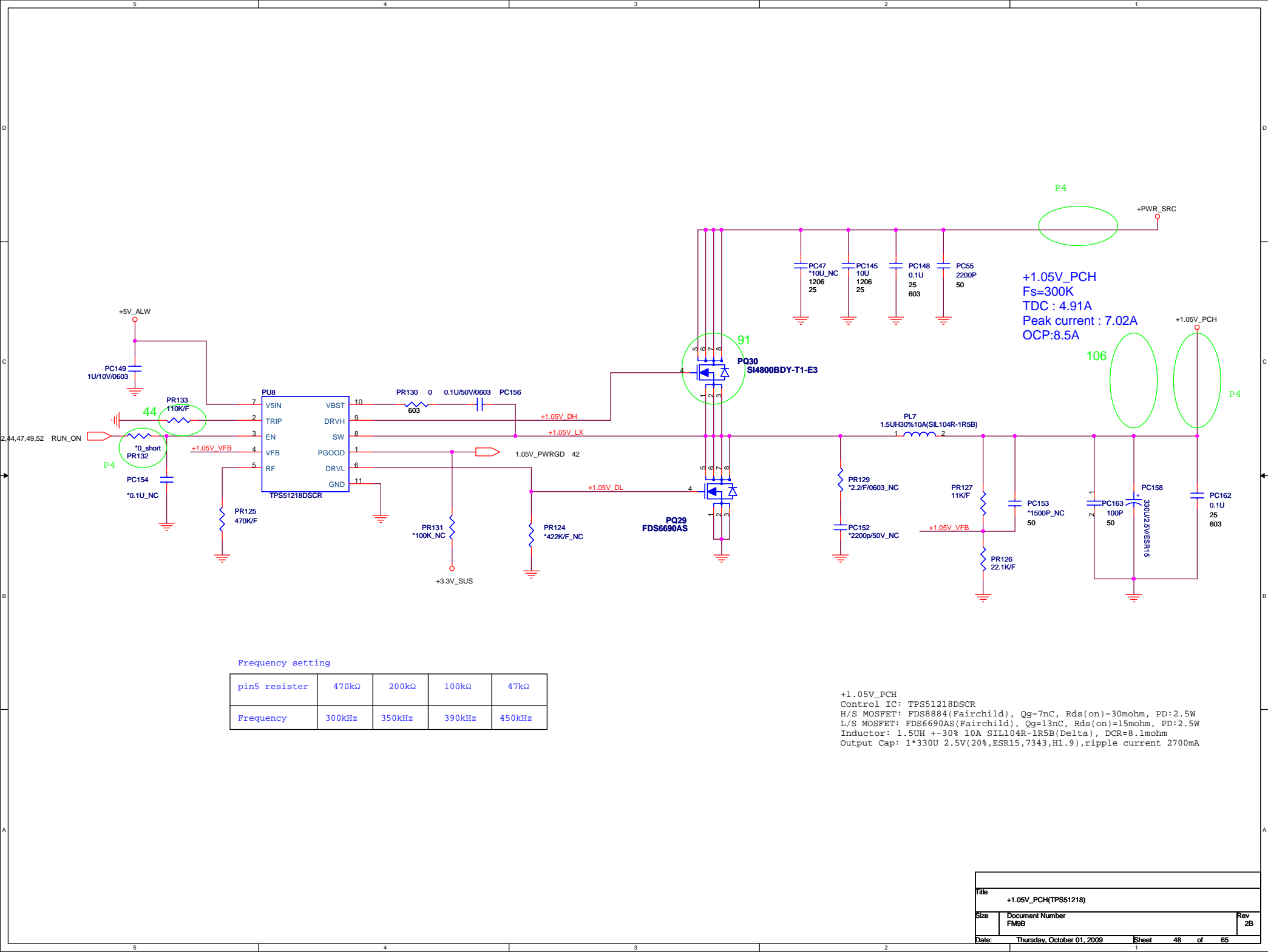
MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

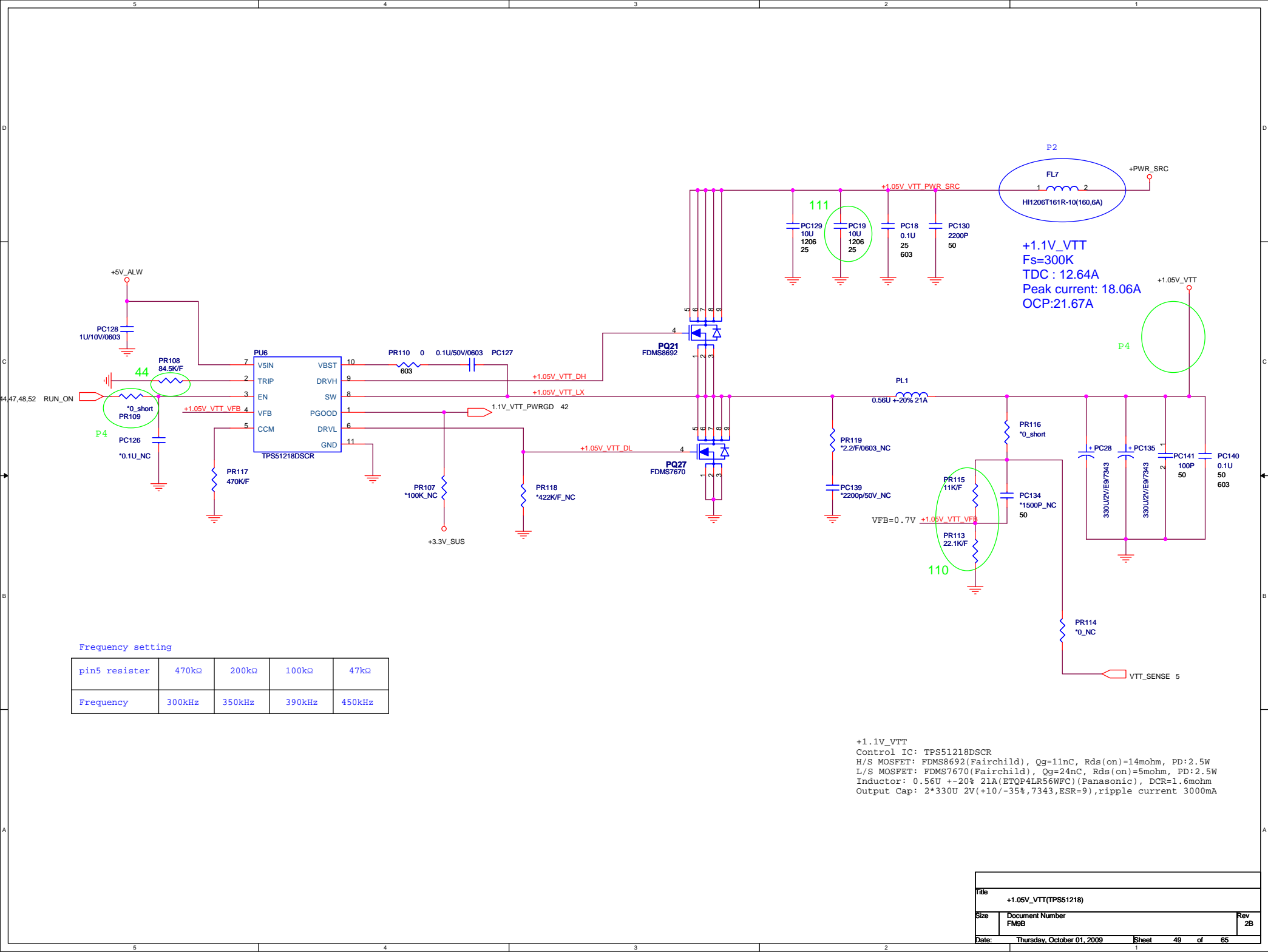
VDDQ output voltage selection

VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	2.5V	VDDQSNS/2	DDR
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)



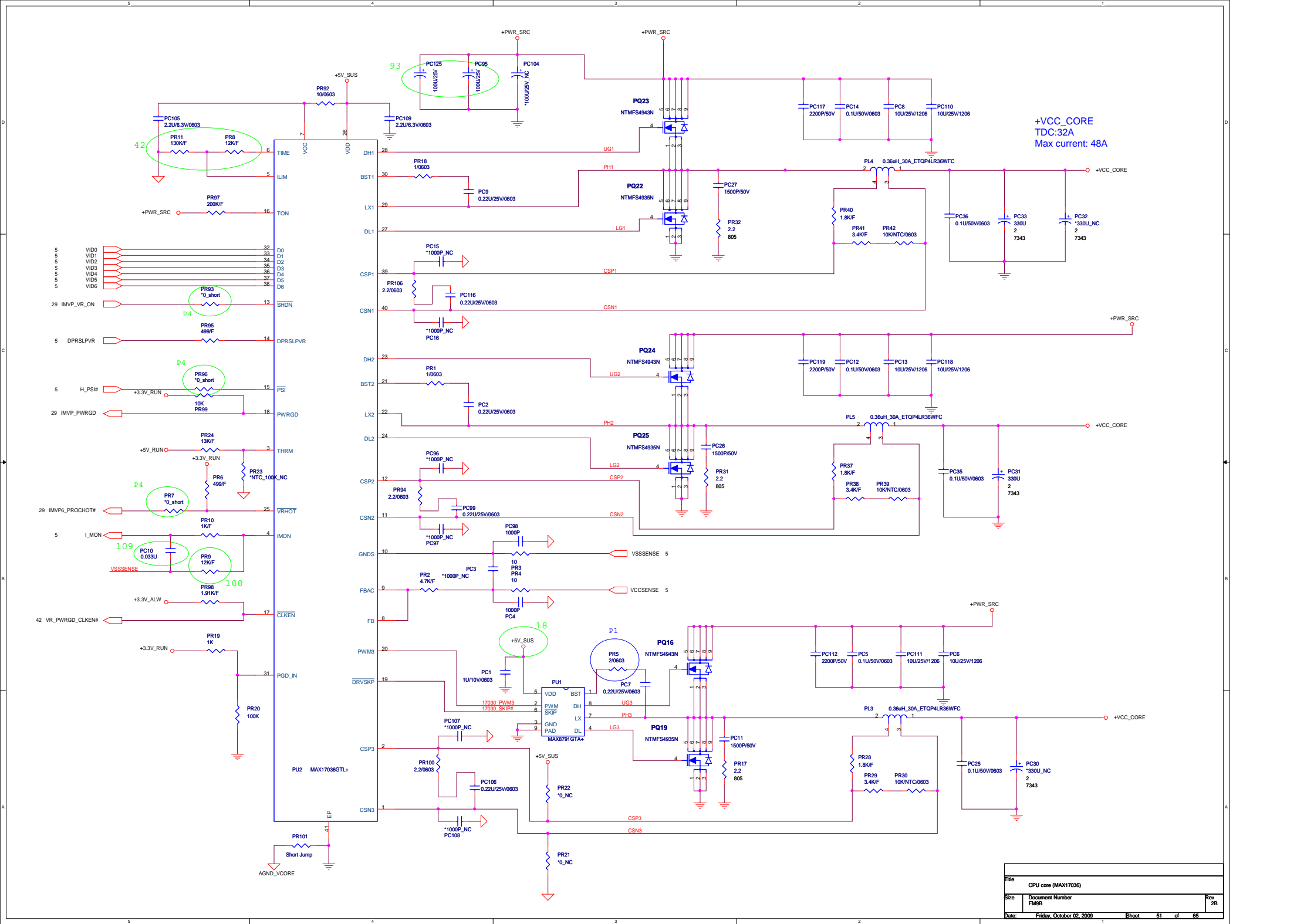


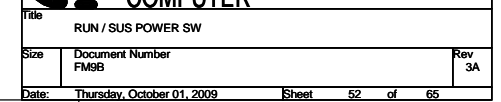
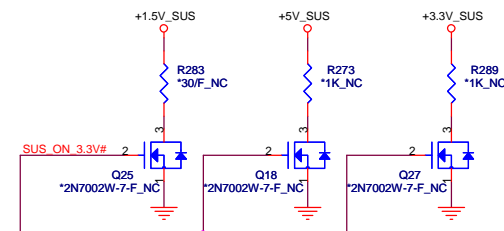
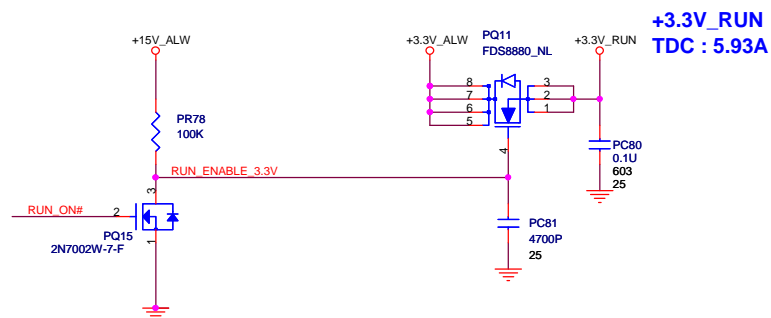
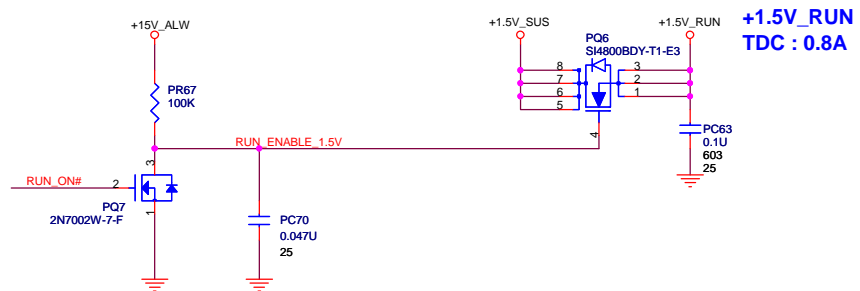
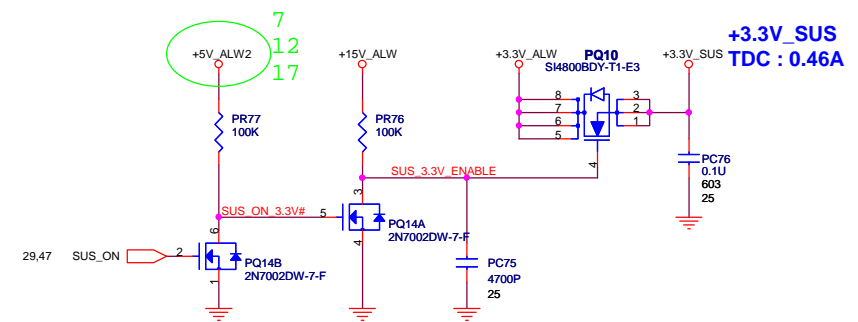
Frequency setting

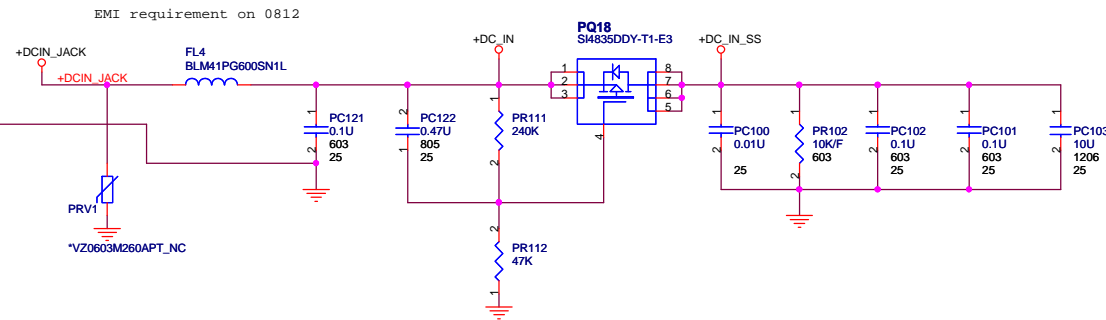
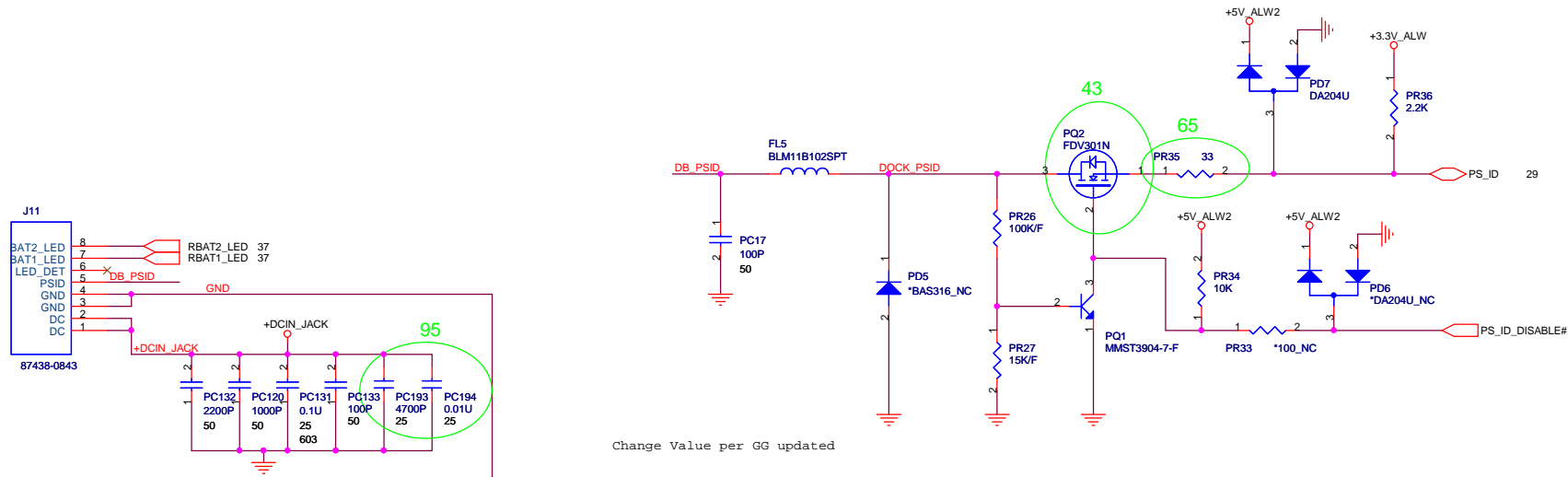
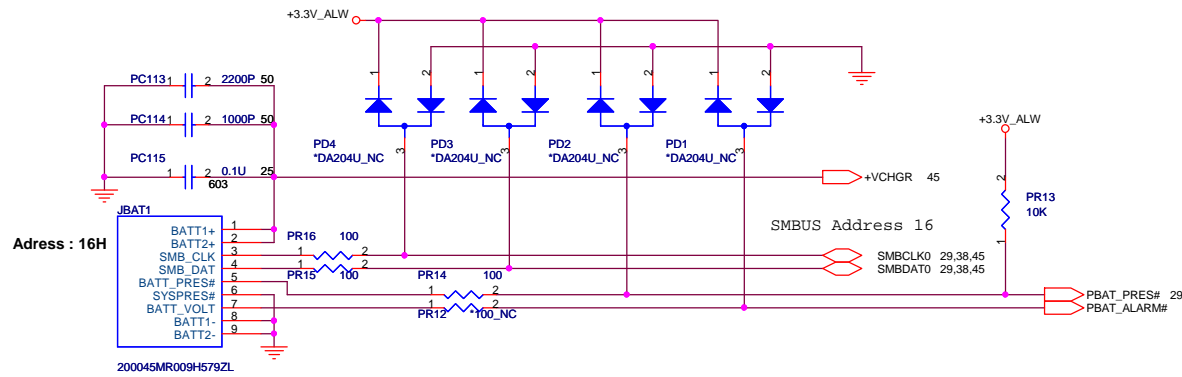
pin5 resister	470kΩ	200kΩ	100kΩ	47kΩ
Frequency	300kHz	350kHz	390kHz	450kHz

+1.1V_VTT
Control IC: TPS51218DSCR
H/S MOSFET: FDMS8692(Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDMS7670(Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
Inductor: 0.56uH +/-20% 21A(ETQP4LR56WPC)(Panasonic), DCR=1.6mohm
Output Cap: 2*3300 2V(+10/-35%,7343,ESR=9),ripple current 3000mA

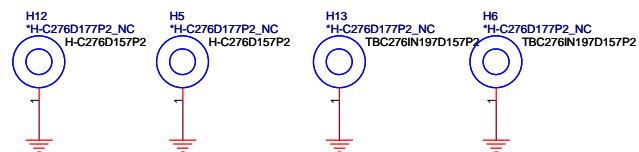
Title			
+1.05V_VTT(TPS51218)			
Size	Document Number		Rev
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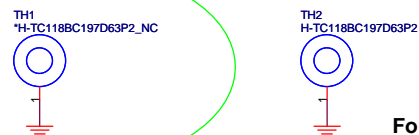




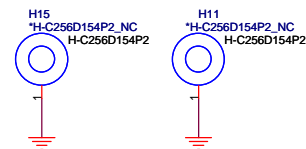
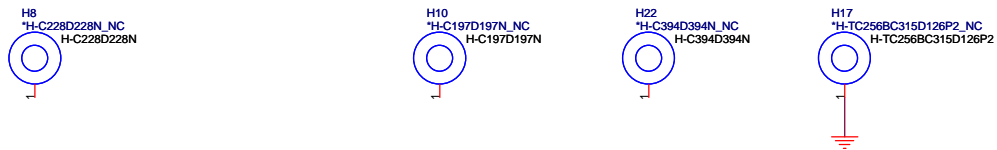
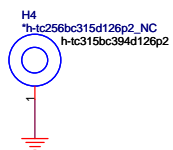
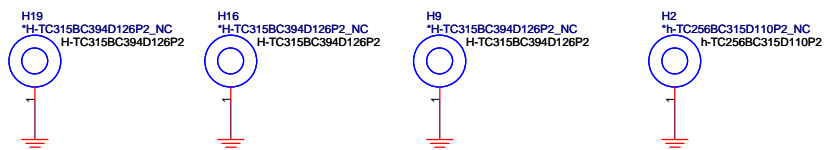
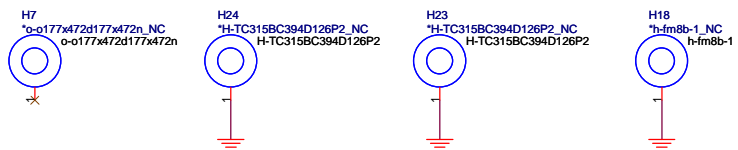
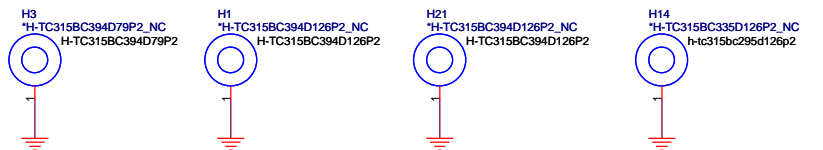
FOR CPU use



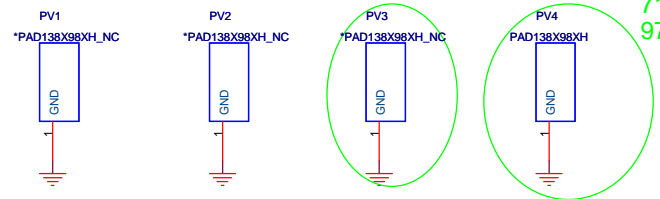
87



For MiniCard nut use.
on 31' header



For PCH nut use.




47

71
97



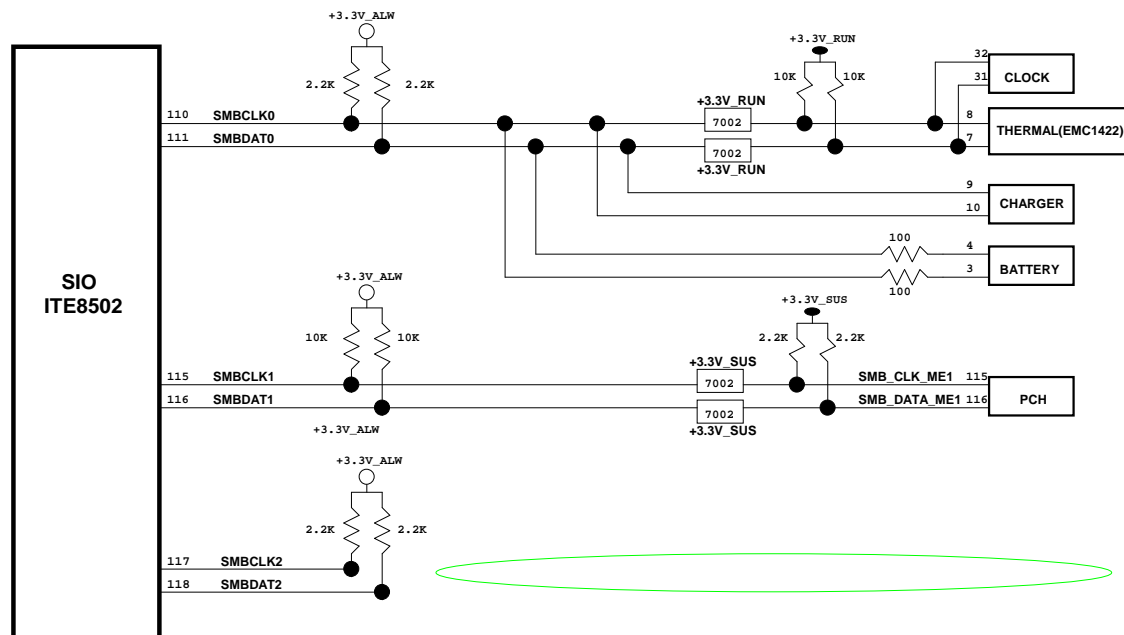
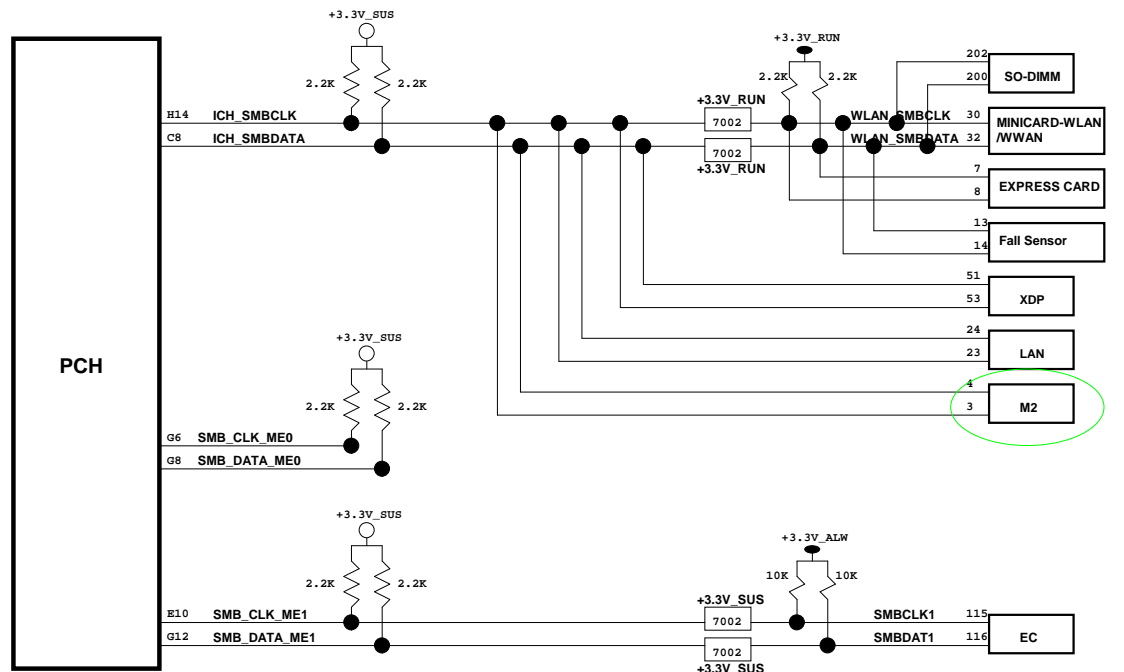
Title			SCREW PAD
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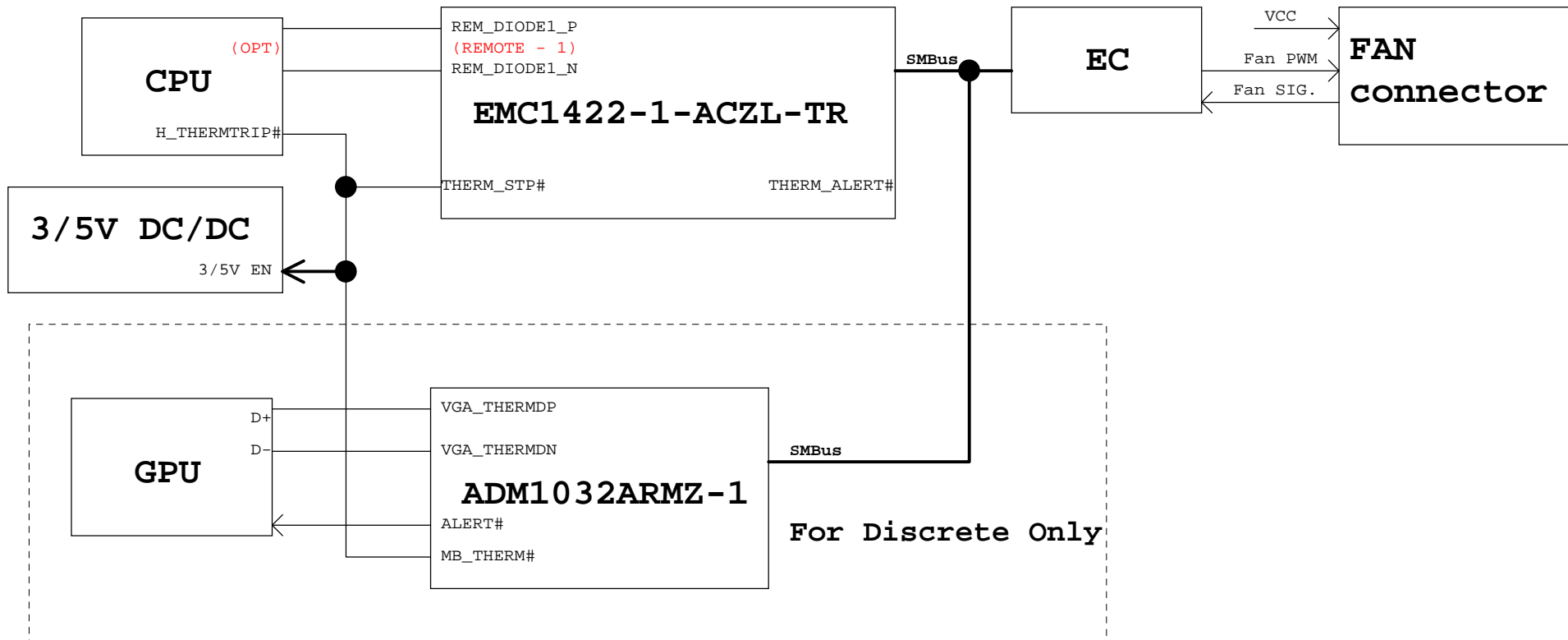
Reserved for EMI.

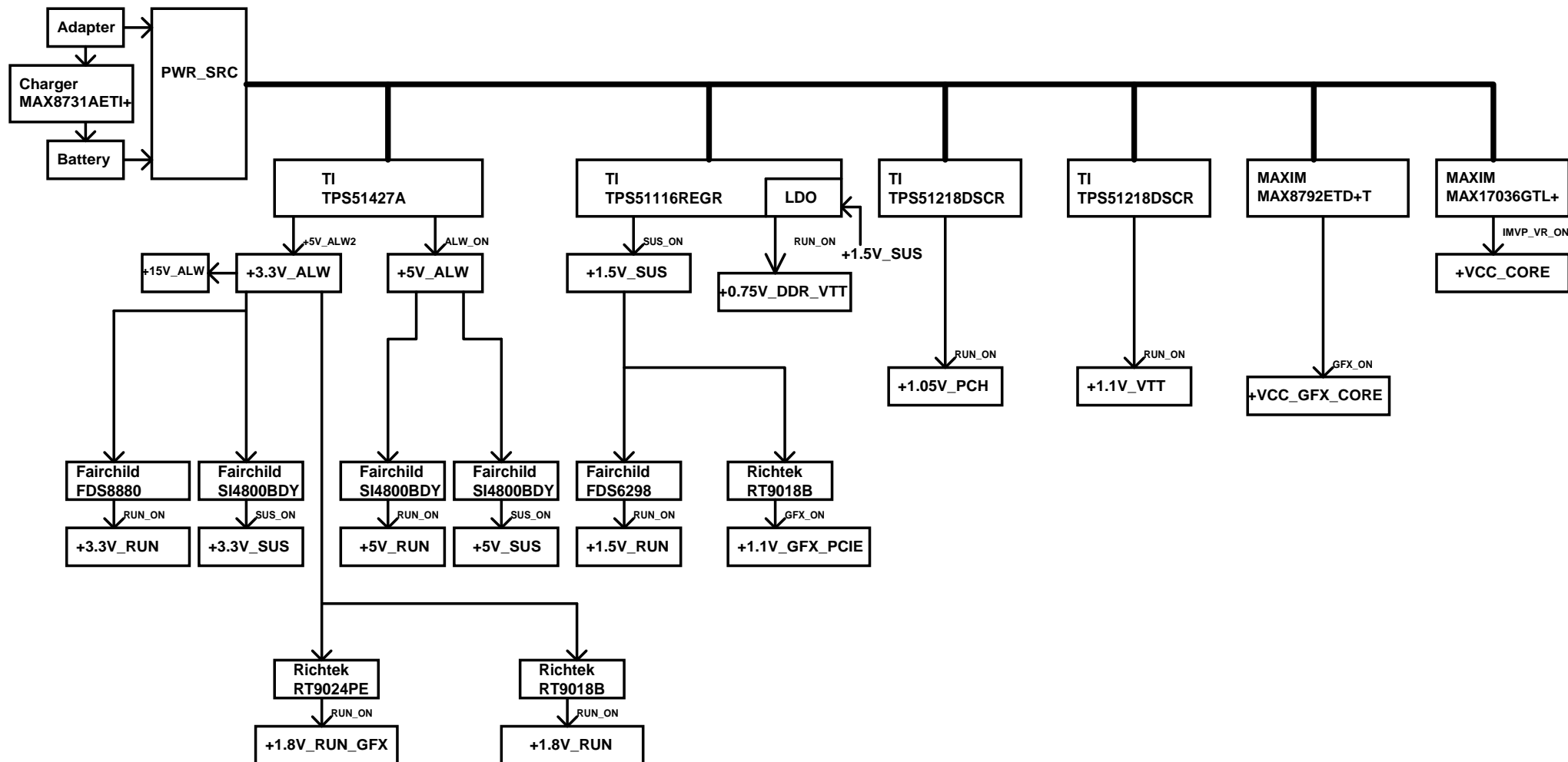


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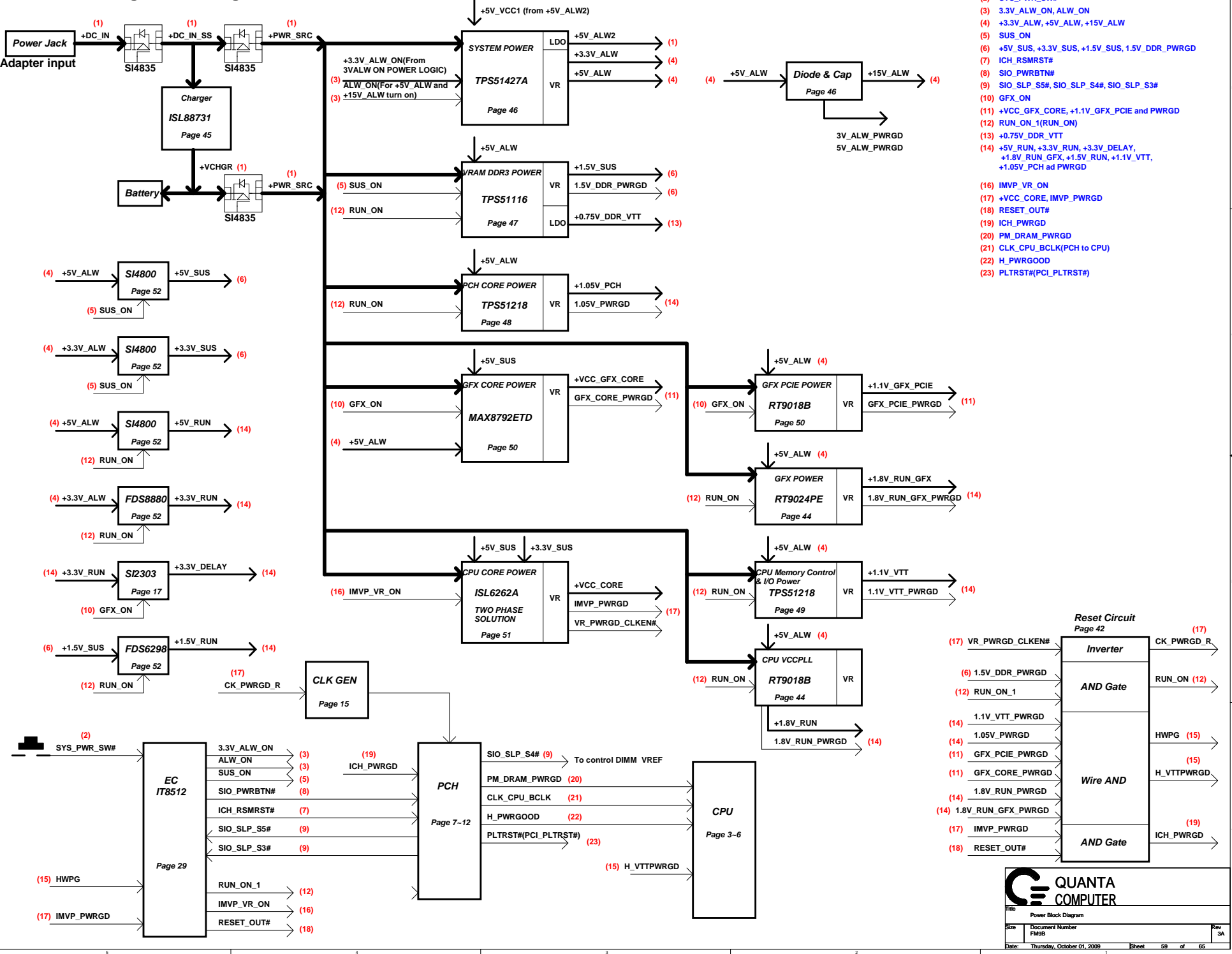
Title		
EMI CAP		
Size	Document Number	Rev
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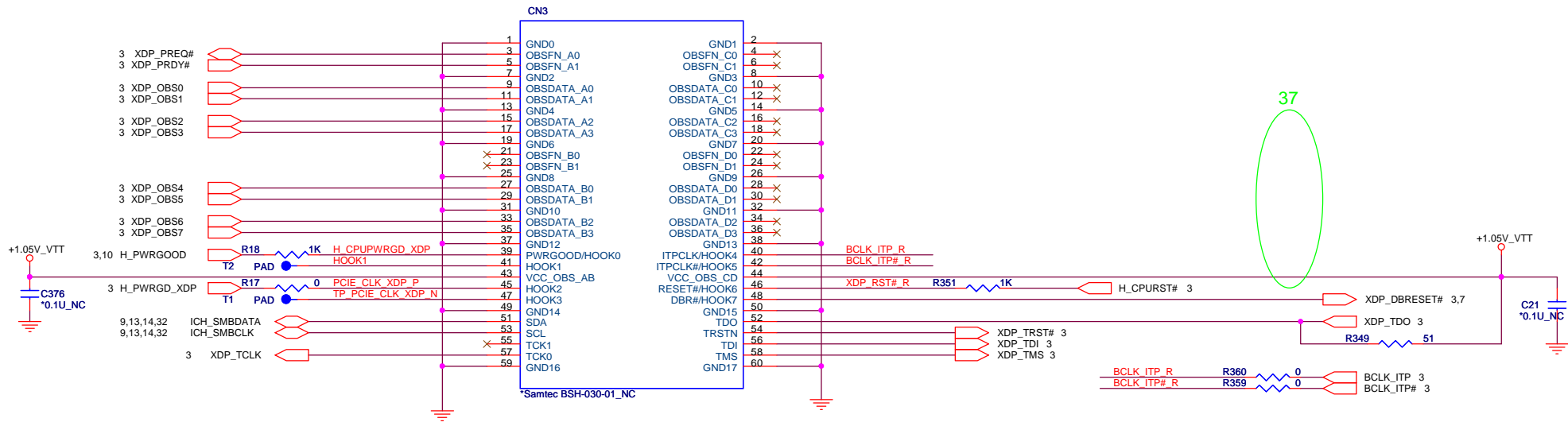







FM9 Power Design Block Diagram 2009/02/25





It is for debug. requesst vendeer provide 200 pcs sample.



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